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Development of a novel micro channel cooling system for the NA62 GTK detector

Doctoral dissertation presented by

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in fulfilment of the requirements for the degree of Doctor in Sciences

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Abstract

NA62 is a Kaon physics experiment whose main objective is the measurement of the rare decay $K^+ \to \pi^+ \nu\bar{\nu}$ (BR$\sim 10^{-11}$). It will be installed at the SPS accelerator at CERN, Geneva. The GigaTracKer (GTK) is a core part of the NA62 experiment. It is a spectrometer made of three semiconductor pixel sensors placed around an achromat magnet. It precisely measures momentum, time and angle of the incoming kaon beam. The GTK setup is placed inside a vacuum chamber, with the main requirement to have minimal material to avoid beam interactions. Per GTK station a total material budget of $0.5\%X_0$ radiation length in beam direction is allowed. This translates into 150 µm of bulk silicon that can be used for cooling the readout electronics. It has to sustain a high and non-uniform beam rate and has to survive in a vacuum and high radiation environment. The dissipated heat produced by the readout electronics is estimated to be approximately 32 W. The maximum allowed operation temperature of the GTK is 5 °C. A lower operation temperature allows for a longer lifetime of the GTK detector and is therefore highly desirable. To avoid a thermal run-away in vacuum a low mass cooling system based on micro channel cooling has been proposed. The micro channel heat sinks are produced with micro fabrication techniques. This means micro channels are etched into a silicon wafer and are closed by bonding a second wafer on top. The objective of this thesis is to design, simulate, test, construct and implement this novel thermal anchoring technique for the NA62 GTK. Two solutions of this novel thermal achoring technique are explored:

1. a silicon micro channel cooling plate with a minimum thickness in the sensitive area (size of the pixel sensor)

2. a silicon micro channel cooling frame that will only cool the outer part of the electronics, which are exterior to the pixel sensor

The silicon micro channel cooling plate has been chosen, by the NA62 collaboration, as the baseline cooling solution for the GTK. The silicon micro channel cooling frame is an alternative solution in case the requirements for the radiation length have to be tightened.

Contents

1 Introduction

1.1 The Scientific Goal of the NA62 Experiment

The NA62 [5] experiment is a fixed target experiment at the SPS accelerator at CERN, the European Organization for Nuclear Research [13]. Its main objective is to find new physics using very rare kaon decays, with branching ratios below 10^{-8}. This kind of decays present some features that make them quite appealing both from the experimental and theoretical point of view.

First of all the kaon system is very well known, with accurate measurements of its fundamental parameters since decades. This is important as the main sources of background in the measurement of rare decays comes from the misidentification of one of the dominant decays. In order to put some order of magnitude to the problem, if we want to measure a branching ratio of the order of 10^{-10}, the rejection of the most probable decays should be at least one order of magnitude less. The so called rejection factors should be of the order of 10^{-11}. There is not a single device in particle physics instrumentation that could provide such a rejection factor. The consequence is that we need to use several apparatus, working at the limit of their performance, in order to achieve such a rejection factor. The exact knowledge of all possible decay channels is essential to arrive to such a performance.

Second, the fundamental interactions, the so called short distance interactions, are quite well known and can be accurately computed. The reason of such lower branching ratios is that that these processes take place in the Standard Model with mechanisms as the Flavour Changing Neutral Currents (FCNC) [52] that are highly suppressed. The control of these short distance effects is extremely important as any deviation from the predicted values in the Standard Model will be a strong evidence of new physics that may appear in loop diagrams.

Besides this short distance contributions these branching ratios are modulated by the long distance contributions that take into account the low energy QCD effects present during the hadronization. These effects are more difficult to compute and usually limit the predictions of these rare decays branching ratios.

Last but not least, from the experimental point of view, the final states coming from kaon decays are relatively simple, with well known topologies and very few particles involved, which ease the particle identification and tracking.

Among rare kaon decays, of special importance are the decays $K^0 \to \pi^0\nu\overline{\nu}$ and $K^+ \to \pi^+\nu\overline{\nu}$. Short distances contributions have been fully computed with two loops electroweak corrections [22] and long distance contributions are under control measuring the QCD matrix elements from the well known decay $K_{\ell 3}$ ($K \to \pi e\nu$). The current prediction for the branching ratios of these channels is exceptionally precise [25]:

- $\mathrm{BR}(K^0 \to \pi^0\nu\overline{\nu}) = (3.00 \pm 0.30) \times 10^{-11}$
- $K^+ \to \pi^+\nu\overline{\nu} = (9.11 \pm 0.72) \times 10^{-11}$

where the major contributions to the error of these branching ratios come from the uncertainty on the CKM matrix elements $|V_{cb}|$, $|V_{ub}|$ and γ.

The strong suppression of the Standard Model contributions and the remarkable theoretical precision of the SM rate means that such decays can be used as sensitive probes for the discovery of new physics effects [59].

In contrast with the theoretical calculations, the experimental knowledge of these decays is less precise:

- $\mathrm{BR}(K^0 \to \pi^0\nu\overline{\nu})_{exp} \leq (2.6 \pm 11)10^{-11}$ [16]
- $\mathrm{BR}(K^+ \to \pi^+\nu\overline{\nu})_{exp} = (17.3^{+11.5}_{-10.5})10^{-11}$ [19].
  On the basis of 7 observed events, the experiment E949 gives a clearly imprecise value. This opens the door to the discovery of new physics beyond the Standard Model [22]

The limit for the $K^0 \to \pi^0\nu\overline{\nu}$ was obtained by the E391a experiment at KEK in 2010. Since May 2013, an improved version of the E391a has been installed at JPARC. This experiment, called KOTO [71], expects to reach the Standard

Model sensitivity by 2020. There are also plans to measure this decay channel at CERN, but this project, if it takes place, will not be before 2020.

The prospects to improve the measurement of the $K^+ \to \pi^+\nu\overline{\nu}$ are more optimistic. Indeed the measurement of this channel is the main objective of the NA62 experiment. The prospect is to accumulate approximately 50 $K^+ \to \pi^+\nu\overline{\nu}$ decay events per year with less than 10% background from 2015-2017, allowing a measurement of this branching ratio better than 10%.

These two channels are without any doubt the best probes for the search of new physics effects, complementary to direct searches, with the advantage of exploring energy scales well beyond the LHC reach. Because of the cleanliness of the theoretical predictions, and assuming a that the current uncertainty will be reduced to $\sim$5%, measured deviations from the Standard Model as low as 20-30% level could be detected with 5σ and, hence, be considered as a signature of new physics. A non exhaustive list of models that could be responsible for new physics effects are:

- Supersymmetric Models Standard Model [18];
- Minimal flavour violation models [74];
- Randall-Sundrum with custodial protection [20];
- littlest Higgs Model with T-Parity [21];
- an extra gauge boson [26].

As said by A. Buras [25]: "Assuming that NA62 and KOTO will reach the expected precision and the measured branching rations on these decays will be at least as high as the ones predicted in the Standard Model, these two decays are expected to be the superstars of flavour physics after 2018". [48].

1.2 The NA62 Experiment

NA62, proposed in 2005 [27], is the latest of a series of experiments (NA31 and NA48 series) at CERN devoted to the study of the flavor structure of the Standard Model with kaons. The common concept of all these experiments is

the use of high energy provided by the SPS accelerator to study the kaon decay in flight.

NA62 experiment can be divided into two stages:

1. 2007 run, which is finished, was a new measurement of the ratio R_K by using the NA48/2 apparatus in 2007. The result of this measurement [38]

$$R_K^{NA62} \equiv \Gamma(K^+ \to e^+\nu)/\Gamma(K^+ \to \mu^+\nu) = (2.488 \pm 0.010)10^{-5}, \quad (1.1)$$

   is the most precise measurement of this ratio so far. It is in good agreement with the value predicted by the Standard Model

$$R_K^{SM} = (2.488 \pm 0.007_{stat} \pm 0.007_{syst})10^{-5} \quad (1.2)$$

   This stage, is now finished.

2. 2014-2017 run focuses on the measurement of the rare kaon decay $K^+ \to \pi^+\nu\overline{\nu}$ with an accuracy of 10%.

To measure the $K^+ \to \pi^+\nu\overline{\nu}$ with this precision, the major sample of K^+ decays ever generated (10^{13} decays) will be studied with a completely new experimental setup that includes the state-of-the-art of particle detection in order to reach the outstanding performances needed.

As a sub-product, the measurement of the rare kaon decay $K^+ \to \pi^+\nu\overline{\nu}$ can be used to make a decisive test of the Standard Model by extracting 10% measurement of the parameter $|V_{td}|$ of the CKM matrix. The Cabibbo-Kobayashi-Maskawa matrix is a unitary matrix, which contains information about the strength of flavour changing weak decays in quarks.

Apart from the study of channel $K^+ \to \pi^+\nu\overline{\nu}$, the 10^{13} K^+ decays are produced. These give the opportunity to study other rare kaon decays with a previously unattained precision. Consequently, the data from NA62 will allow a number of interesting studies of different channels of kaon decays.

1.2.1 The Experimental Strategy and Setup

The kaon decay in flight $K^+ \to \pi^+\nu\overline{\nu}$ produces a positively charged pion and two undetectable neutrinos, see figure 1.1. Therefore the signature of the signal consists of a single π^+ track reconstructed downstream of the decay volume and matched to a K^+ track upstream and the missing mass. The design of the experiment requires a redundant measurement of the event kinematics and hermetic vetoes to achieve a background rejection of $S/B \simeq 10$. The design of the experiment guarantees the rejection factor of 10^{12} between the signal and the other K^+ decay modes, see figure 1.2.

The experiment relies on the following factors to achieve the required level of background rejection with respect to the signal channel [5]:

- high-resolution timing - to match the high-rate of incoming particles (750 MHz);
- kinematic rejection - to identify pions coming from the original particle beam and not from the wanted kaon decay;
- particle identification of kaons, pions, muons, electrons and photons;
- hermetic vetoing of photons out to large angles and of muons within the acceptance.

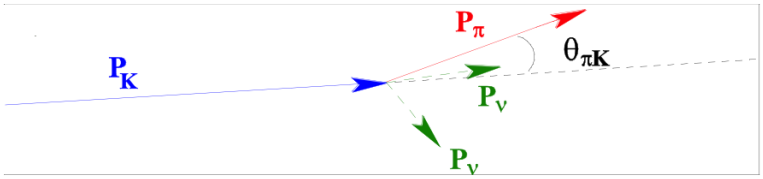


Figure 1.1: Kinematic of the $K^+ \to \pi^+\nu\overline{\nu}$ decay

The high energy of the proton beam, used in the experiment has two effects.

First, the Kaon decay will take place in the forward region. Consequently, the instrumentation can be concentrated in this region. This helps to hermetically cover the decay region and to minimize zones without instrumentation.

Second, the particles created by the decay have enough energy to be detectable in the forward region.

The incoming kaons are measured in the Gigatracker sub-detector. The charged products of the decay are measured by the straw-chamber spectrometer and are identified in the Ring Imaging CHerenkov (RICH) sub-detector and the MUon-Veto (MUV) sampling calorimeter. The LKr calorimeter, originally built for NA48, identifies and vetoes the forward photons. Photons at large angles are identified by a series of 12 ring-shaped Large Angle Veto counters (LAV), using lead-glass blocks.

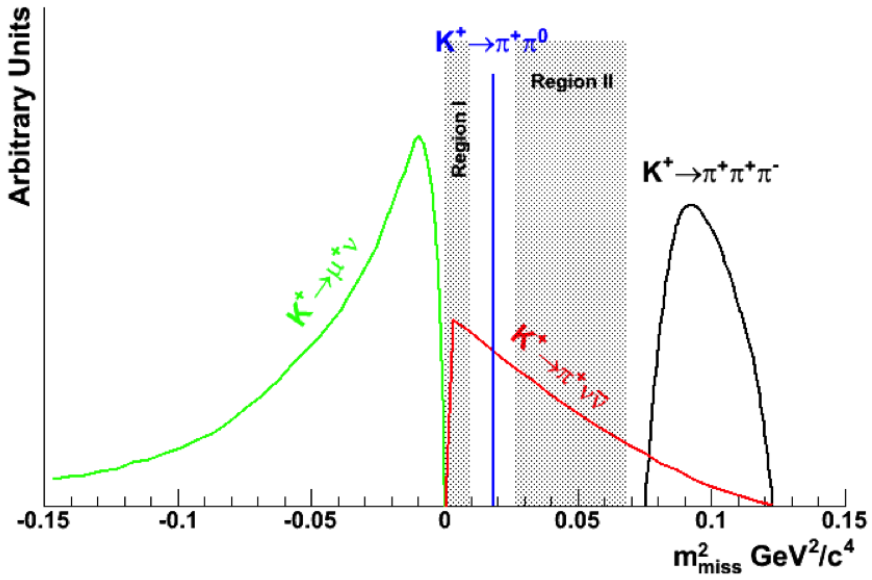


Figure 1.2: Distribution of the missing mass of the $K^+ \to \pi^+ \nu\bar{\nu}$ decay and dominant background

The experiment needs tracking devices for both K^+ and π^+, and also calorimeters in order to exclude photons, positrons and muons. Additionally, the experiment needs particle identification systems to identify the incident kaons and to distinguish π^+ from μ^+. e^+ must also complement the tracking and veto detectors to reach the ultimate sensitivity and to guarantee redundancy. The guiding requirements for the construction of the NA62 detectors are therefore:

accurate kinematic reconstruction, precise particle timing, efficiency of the vetoes and excellent particle identification. Figure 1.3 shows the principle layout of the experiment.

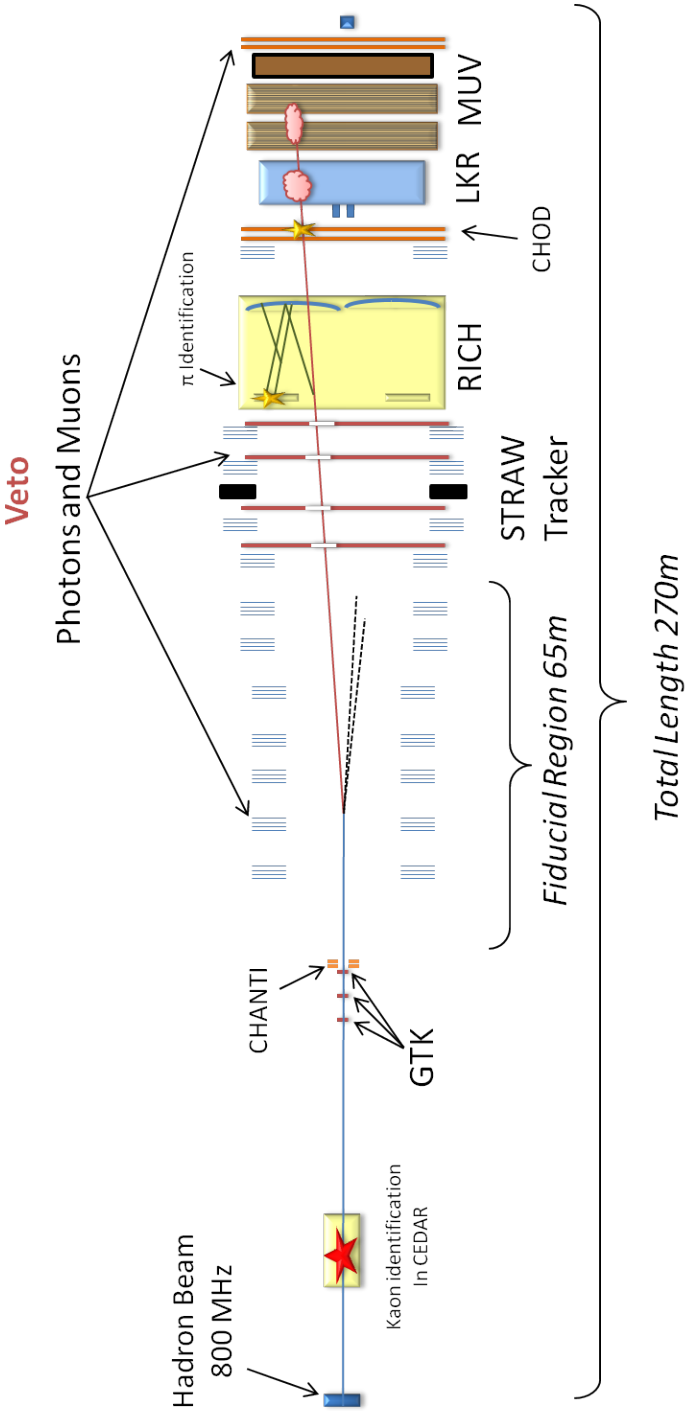


Figure 1.3: Schematic view of the NA62 experiment [59].

1.3 The GigaTracKer Subdetector

The GigaTracKer (GTK) is a core part of the NA62 experiment. It is a spectrometer that provides precise measurements of momentum, time and angle of the incoming 75 GeV/c kaon beam. Beam measurement is essential for the selection of the $K^+ \to \pi^+\nu\overline{\nu}$ decay. The Gigatracker is composed of three stations (GTK1, GTK2 and GTK3) mounted around four achromat magnets as shown in Figure 1.4 [59].

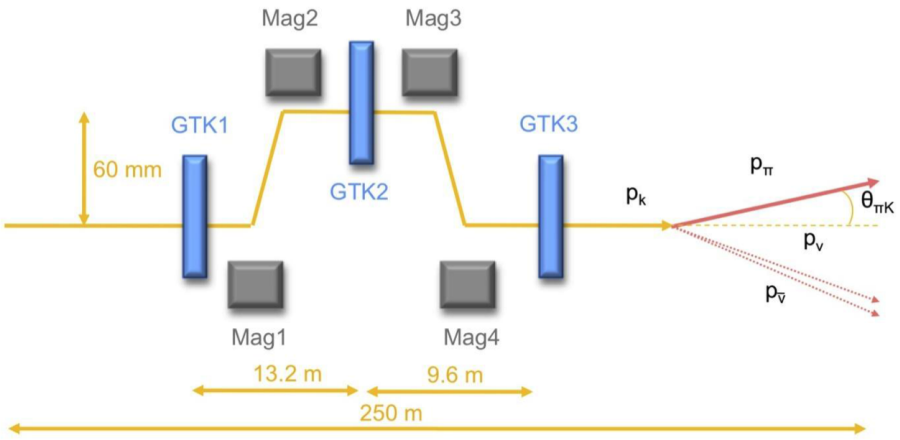


Figure 1.4: Layout of the GTK stations

This setup is placed along the beam line inside the vacuum tank, just before the fiducial region in the decay vacuum pipe. It has to sustain a high and non-uniform beam rate and to survive in a high radiation environment. The pixel size of 300 µm x 300 µm is sufficient to achieve an excellent spatial resolution. Figure 1.5 shows a naive schematic layout of one GTK module.

The GTK beam spectrometer has to sustain a high and non-uniform beam rate of 0.75 GHz in total, hence the name Gigatracker, with a peak of 1.3 MHz/mm^2 around the centre. To meet the resolution requirements the beam spectrometer is installed in a vacuum with a minimal amount of material interaction with the beam to preserve the beam divergence and to limit beam hadronic interactions. The spectrometer is composed of three hybrid silicon pixel stations. Each station is made of one hybrid silicon pixel detector with a total area of 63.1 mm x 29.3 mm containing 300 µm x 300 µm pixels arranged in a matrix of 90 x 200

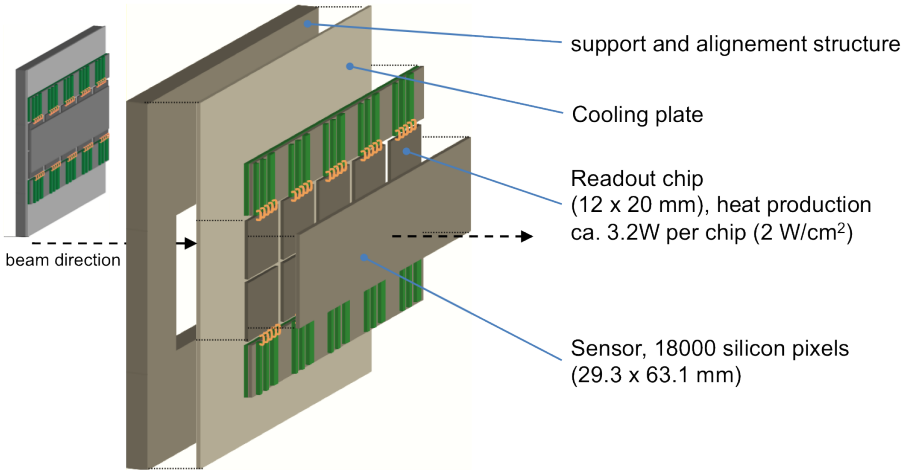


Figure 1.5: Schematic view of one GTK module

elements. With this configuration the detector matches the expected beam dimensions of ca. 60 mm x 27 mm. The pixel dimensions and the distances between stations are adapted to deliver the required momentum and direction resolution [59].

The amount of material crossed by the beam at each station influences the angle measurement. The chosen sensor thickness of 200 µm corresponds to 0.22 % of a radiation length, X_0. The design efforts take into account the optimal minimization of material, as the physics performance strongly depends on a low material budget. Imposing an equivalent material budget to the read-out and cooling system, the total amount of material per station is required to not exceed 0.5 % X_0. Furthermore, due to the high intensity, the required time resolution on every single track using all three stations is 150 ps [59].

The expected fluence in the central region of the sensor is 2×10^{14} 1MeV n_{eq}/cm^2 for a typical 100-day run time year. This value is comparable to fluences expected in the inner layers of the LHC trackers over ten years of operation and requires the sensors and the application specific integrated circuits (ASIC) to cope with the high radiation environment. In order to reduce the radiation induced leakage current on the relatively large sensor the operating temperature is set to 5°C or below. The very low mass of the detector, the operation in vacuum and the need to limit the leakage current due to radiation damage

demands a very efficient and reliable cooling system [59].

1.4 Cooling Requirements

The cooling design is driven by the following unique requirements of the GTK subdetector:

- Material budget:
  - radiation length in active beam area $\leq 0.5\,\%$ of X_0,
  - minimum amount of material in the sensor area (60 mm x 27 mm) plus a 10 mm safety zone,
  - outside that zone no material budget constraints.
- Detector operating temperature 5°C or lower;
- Temperature uniformity of the pixel sensor $\pm 3\,^{\circ}$C or less;
- Power consumptions per GTK station of approximately 32 W;
- System operating in vacuum.

Thermal run-away and destruction needs to be avoided due to the low mass of the detector module. The cooling system for the Gigatracker reduces the radiation damage of the sensor and consequently increases the module life time. Although the upper limit of the operation temperature has been set to 5°C, a lower operation temperature is highly desirable, as the module life time would increase from 50 days to 100 days when cooled at -20°C.

The material budget and the operation in vacuum are the main integration challenges of the project. Mechanics and cooling integration can benefit from the fact that no material budget restrictions exist beyond 10 mm from the pixel sensor. From the perspective of cooling performance the anticipated $2\,\mathrm{W/cm^2}$ heat dissipation by the active electronics are not difficult to meet. However, the cooling and mechanics support architecture must introduce only a minimum of material into the beam area and at the same time assure mechanical stability

of the module and allow access to high speed electrical connections. The working group has considered two independent options: 1) a micro channel heat exchanger with liquid cooling; 2) a gas cooling vessel with thin mylar walls in the beam region with a high velocity nitrogen gas flow [59].

Following the decision of the working group to proceed with the development of the End-of-Column chip architecture, the micro channel heat exchanger was chosen to cool the GTK. The EoC design has regions with different heat flux density. The regions with a high heat flux density can not be cooled with the gas flow as proposed in the second cooling option. Tests in the gas cooling vessel showed temperature differences up to 70 °C on the electronic mock-ups. The temperature differences during start up and shut down of the cooling and the electronic mock-ups were even higher. Only a liquid coolant flow in direct contact with the readout chip, like in the first option, can sufficiently transport this heat away.

The outstanding cooling performance and its low mass are the key features making micro channels a very attractive technology for particle physics detectors. Research on micro channels is needed to adapt this technology to various applications.

The engineering and scientific part of the thesis work consists of

1. the conceptual and engineering design of a cooling system comprising a vacuum vessel housing the detector in the beam
2. the hydraulic and thermal layout of the micro channel heat sink and its manifold system, using analytical methods and numerical simulations (ANSYS, CFX)
3. the follow up of the prototype production of the micro channel heat sink at the clean room of EPFL in Lausanne
4. the designs for the interfaces, distribution systems and instrumentation
5. the building of a test setup to measure the hydraulic and thermal performance of the micro channel heat sink under conditions close to those of the real experiment (heat load, vacuum...)
6. the contribution to the design and production of a heater mock-up that resembles the final sensor assembly as closely as possible

7. the development of the integration process of a sensor assembly, a micro channel heat sink, a carrier board and a vacuum flange

The results shown in the following chapters promise a successful implementation of the micro channel cooling techniques in future HEP experiments, e.g. the silicon tracking detectors of the LHC experiments CMS and ATLAS.

2 Cooling Systems Overview

The GTK silicon pixel detector has unique requirements with respect to the cooling system. The most critical constraints are the extremely low material budget and the operation in vacuum. The vacuum excludes the possibility to cool with a forced convection of gas. The low material budget limits the cooling via thermal conduction through a solid material. This chapter briefly presents the basic principles of heat transfer used in the cooling of electronics in High Energy Physics (HEP), cooling solutions for silicon tracking detectors and the methods used to produce a layout of the micro channels used to cool the GTK.

2.1 Cooling of ASICs in HEP

Application Specific Integrated Circuits, ASICs, are used in HEP to process the signals coming from the sensor. Therefore they are very close to the sensors of the detectors, which means their thermal performance influences the sensors. Traditionally they are cooled via thermal conduction and thermal convection. The heat produced in an ASIC (heat source) is conducted into a heat spreader, usually a metal with high thermal conductivity, with a large heat exchange surface. The heat is then transferred to the surrounding atmosphere via natural thermal convection or forced thermal convection. This cooling technique is not only used in particle physics experiments, but also in devices like laptops, desktop personal computers and also in large computer centres.

2.1.1 Thermal Conduction

The heat flow through a homogeneous and isotropic solid element, with the length L and the uniform cross section A, with neither heat source nor heat

sink and in steady state condition ($\frac{dT}{dt} = 0$), is calculated according to Fourier's law [47] as

$$\dot{Q} = \frac{A}{L} \int_{T_1}^{T_2} k(T) dT = \frac{A}{L} \bar{k} \Delta T. \tag{2.1}$$

T_1 and T_2 are the temperatures at both ends of the element and $k(T)$ is the temperature dependent thermal conductivity of the material. The right side of equation (2.1) shows that one can define a mean thermal conductivity $\bar{k}$ for a specific temperature range. The heat flow $\dot{Q}\,[W]$ through a solid element depends linearly on the temperature gradient ΔT, the reciprocal of the length L, the cross sectional area A and its mean thermal conductivity $\bar{k}$. The thermal conductivity only depends on the bulk material and its temperature, while its pressure dependence is insignificant for solid materials.

Due to the heat flow dependence on length and cross section of the heat conducting solid, the cross section needs to be larger for a longer path of conduction. In High Energy Physics (HEP) applications this would lead to the use of additional material for long conduction. That is why it is necessary to keep the conduction length as short as possible and transport the heat away using a flowing fluid.

2.1.2 Thermal Convection

Convective heat transfer can only occur in fluids. It superimposes the two mechanisms of diffusion and advection. Diffusion is the molecular heat conduction inside a fluid (2.1.1). Advection is the macroscopic motion of the fluid that transports the heat with it [46]. In the presence of a temperature gradient, such a motion causes a heat transfer. Depending on the properties of the fluid and the nature of the flow, the heat transfer is dominated by one of these mechanisms. In heat and mass transfer, the sum of the diffusive transfer and advective transfer is called convection.

Of special interest is the convective heat transfer between a moving fluid in direct contact with a fixed surface at a different temperature. This process occurs in all heat exchanges, where a fluid in motion transports heat away from a solid heat source, which is the case in most tracking detectors in HEP.

To describe the heat transfer on a surface, we use a formula that corresponds to Newton's law of cooling [60]:

$$\dot{Q} = Ah(T_S - T_\infty). \tag{2.2}$$

T_S is the surface temperature and T_∞ is the bulk fluid temperature. A is the surface involved in the heat exchange. The parameter h ($\mathrm{W/m^2 \cdot K}$) is named convective heat transfer coefficient. The coefficient depends on the conditions in the boundary layer of the fluid, the surface geometry and the thermodynamic properties of the fluid.

For a given temperature difference $(T_S - T_\infty)$, the heat flow $\dot{Q}\,[W]$ to the fluid can be raised by increasing the heat exchange surface A and by influencing the flow conditions in the boundary region, hence raising the convective heat transfer coefficient. In particular, the transition from laminar to turbulent flow conditions raises the heat transfer coefficient significantly. In laminar flow conditions, diffusion dominates the heat transfer, while advection dominates in turbulent flow conditions. The transfer from laminar to turbulent flow is connected to a rise in the flow velocity, which leads to a higher pressure drop.

With micro channels the goal is to reduce the amount of material installed in particle direction of HEP tracking detectors. The minimization of the channel dimensions in a micro channel leads usually to laminar flow conditions in the micro channel heat exchanger. Therefore the heat exchange surface A is increased to a maximum with multiple parallel micro channels.

2.1.3 Thermal Radiation

Thermal radiation is fundamentally different from thermal conduction and thermal convection. The heat flux through conduction appears in solid, liquid and gaseous matter as a vector connected to the temperature gradient. In addition, heat appears in matter as the kinetic energy of the molecules. In contrast, the thermal radiation on a point is independent of the temperature of the matter at this point. A good example is the thermal radiation coming from the sun. On its way to earth, it passes interstellar space with a temperature close to

absolute zero, while the sun's surface temperature is 5778 K and the earth's mean surface temperature is 288 K [39].

Thermal radiation is energy emitted by matter with a temperature above absolute zero. The radiation energy is transported by electromagnetic waves, which originate from the thermal energy of the matter's surface. The heat flow $\dot{Q}\,[W]$ emitted by a body can be calculated using the Stefan-Boltzmann-law [46]:

$$\dot{Q} = \epsilon \sigma A T^4. \tag{2.3}$$

Where ϵ is the emissivity of the surface, σ is the Stefan-Boltzmann constant ($5.67 \times 10^{-8}\,\mathrm{W/m^2 \cdot K^4}$), A is the surface area and T the temperature of the body. The emissivity has a value between $0 \leq \epsilon \leq 1$ and gives a measure of how efficiently a surface emits energy relative to the surface of a black-body ($\epsilon = 1$).

The heat exchange between two or more surfaces through thermal radiation depends strongly on the surface geometries and orientation, as well as on their radiative properties and temperatures. In the cooling of HEP tracking detectors thermal radiation can be neglected. This is because of the small heat flow $\dot{Q}\,[W]$, compared to conduction and convection. The small temperature differences, confined spaces and small surfaces, that are intrinsic to tracking detectors, restrict the possible heat flow.

2.1.4 Phase Transition

A special case of heat transfer occurs in fluids when they change their aggregate state. The phase transition from gas to liquid is called condensation and for liquid to gas it is called evaporation. Naturally a cooling liquid changes to the gaseous state, since this transition absorbs heat. The heat transfer between a solid and an evaporating cooling liquid is still governed by thermal convection and conduction inside the liquid phase. This is true as long as the solid walls are covered by a liquid film. If the solid walls get into contact with the gas phase the heat transfer suddenly drops dramatically. This is called a dry out.

For the cooling of HEP detectors, two-phase cooling is of high interest, since large quantities of heat can be removed with a small mass flow. This translates

into a minimal amount of material needed for cooling inside of the detectors. An evaporating mass flow of C_6F_{14} absorbs about 80 times the thermal energy that the same mass flow absorbs, when its temperature rises by one degree Celsius. And an evaporating mass flow of CO_2 can absorb about 250 times the thermal energy compared to the same mass flow of CO_2 with a temperature rise of one degree Celsius. Several HEP experiments use already two-phase cooling, e.g. AMS and LHCb with CO_2 cooling circuits [83] and ALICE with a C_4F_{10} cooling circuit [37]. These experiments use cooling tubes connected to a heat spreader that collects the heat from the readout electronics.

Parallel micro channels used for detector cooling need a special design to work with two-phase cooling. It needs to be ensured that the cooling fluid enters each channel in liquid state. A liquid entry into a channel can be reached with a pressure drop or a temperature rise of the cooling liquid at the beginning of each individual channel. Evaporation in the inlet manifold would lead to maldistribution of the cooling fluid and blocking of channels by gas bubbles. Consequently a uniform temperature distribution of the micro channel heat sink could not be guaranteed. These difficulties lead to the decision to abandon two-phase cooling for the cooling of the GTK sub-detector.

2.2 Cooling of HEP Silicon Tracking Detectors

Silicon tracking detectors belong to the large family of ionisation detectors, which are based on the movement of free charges in an electric field. They use the same effect as gas and liquid Argon detectors, but are based on a solid material and on the principle of a reverse biased junction diode. A particle passing through silicon creates roughly 8000 electron/hole pairs per 100 µm path length. An electric field separates the produced charges and gives a measurable induced current on the electrodes [41].

The fixed target experiment NA11 at CERN was one of the first experiments to use a silicon strip detector to measure the momentum, time and angle of a particle beam. Since then silicon tracking detectors became widely used as tracking and vertex detectors in HEP, e.g. all 4 LEP experiments upgraded to silicon tracking detectors during their lifetime. They are now state of the art in track detection, which is documented by the fact that the LHC experiments

ALICE, ATLAS, CMS and LHCb widely use silicon strip and silicon pixel detectors for tracking. With the use of silicon detectors, which require electricity to power an electrostatic field and the readout electronics, in the confined space of experiments on particle colliders, cooling has become an important part of the detector development [43].

The cooling of HEP silicon tracking detectors faces peculiarities that are unique and therefore require dedicated research and development. Important points to consider are:

- Operation under a strong magnetic field, e.g. up to 4 T in the CMS experiment [30];
- Operation in high radiation environment, $\gtrsim 10^{14}$ n_{eq}/cm^2 in one year of operation;
- Operation in vacuum or controlled environment to insulate from external heat and to avoid condensation;
- Accessibility is generally limited to long shutdowns [1];
- Low mass of cooling equipment to avoid interactions of particles with matter.

These boundary conditions lead to limitations in the design process. The materials used have to be non-magnetic to avoid movement in components. Materials have to withstand high radiation without disintegration or rapid ageing. This is especially important in the choice of the coolant and the heat spreader. Vacuum or a controlled environment and the complex geometries limit the possibilities to cool via convection. Cooling via radiation is excluded since it needs large surfaces and high temperature differences to cool effectively.

2.2.1 Evolution of Silicon Detector Cooling

As previously mentioned, cooling has become important in silicon detectors in collision experiments, since readout electronics and consequently also cooling needs to be integrated into the detector design. Here the distinction should be made between silicon strip and silicon pixel detectors.

[1] Maintenance interventions of 2 month or more, that require a stop of the accelerator.

In silicon strip detectors the readout electronics can be placed at the end of a strip, hence outside of the sensitive area of the silicon and therefore do not add to the material thickness of one detector module. Nevertheless, the material is next to the detector module and can influence the particle trajectories in subsequent outer layers via multiple scattering. In silicon pixel detectors on the other hand, the readout electronics are bump bonded under the sensitive pixels. As a consequence both the electronics and the cooling add to the total material of a single detector module.

The experiments on colliders enclose the interaction point with several layers of modules. The thickness of each module influences the signals in outer layers. The active silicon area, mentioned later, is the sum of the sensitive silicon strips and pixels. It does not include the readout electronics.

The readout of the signals of the NA11 silicon strip detector was realized with external devices connected via long cables, see Figure 2.1. This meant that the cooling of these readout devices could be realized independently from the actual detector and did not influence its performance. In contrast, the silicon vertex detectors in collision experiments need cooling of the silicon sensors and the integrated readout electronics close to the interaction point. Figure 2.2 shows the complexity of a module of the CMS pixel detector. Cooling tubes still need to be thermally connected to the module.

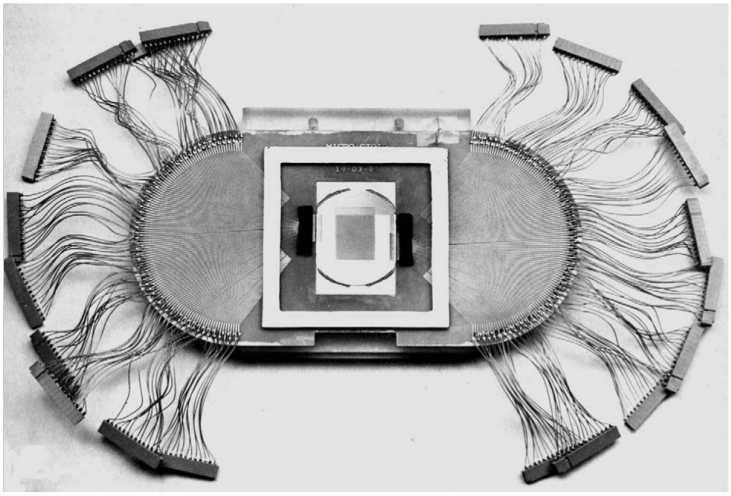


Figure 2.1: A mounted NA11 silicon strip detector [81].

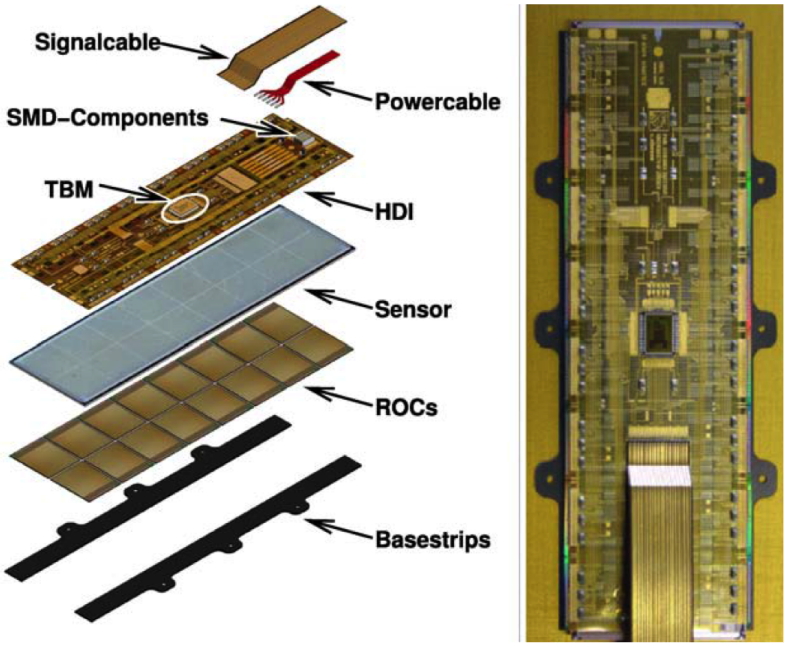


Figure 2.2: A CMS inner tracker pixel module [30].

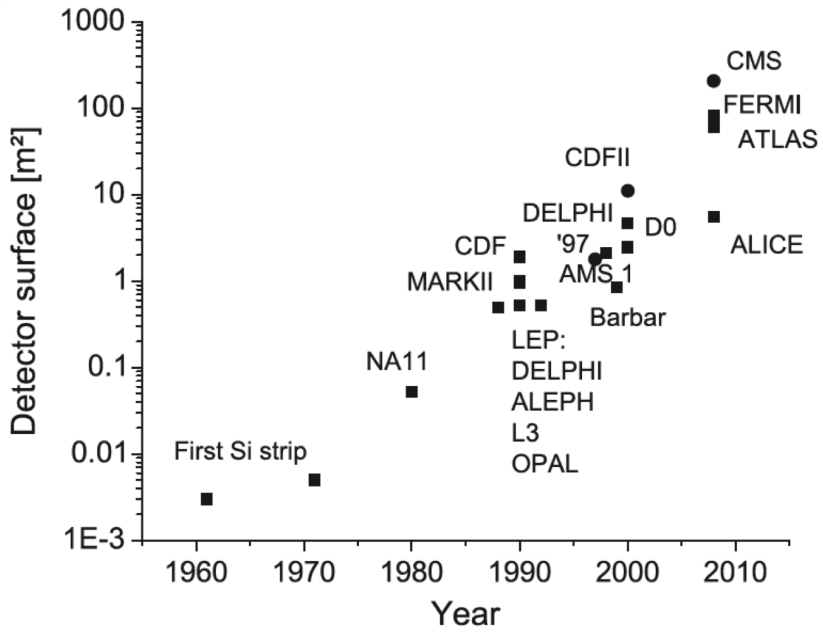


Figure 2.3: The increase of installed active silicon surface over the last decades strikingly proves the importance of silicon detectors in HEP and the rising needs for cooling [42].

Figure 2.3 illustrates the growing importance of silicon tracking detectors in HEP. During the last three decades all major physics experiments used silicon strip and silicon pixel detectors to measure particle tracks. The installed active silicon surface in the CMS experiment compared to the the Delphi experiment in 1990 is three orders of magnitude larger. The evolution of silicon tracking detectors tends to larger sensors and more layers. It means that the geometries become more complex and packed. Furthermore the detector designs need to become lighter to avoid increased particle interaction with matter. CMS is the first HEP experiment to use silicon strip and silicon pixel sensors exclusively in its tracking detector.

Table 2.1 illustrates the evolution of silicon tracking detectors on the example of three experiments, Delphi [34, 77], BaBar [76, 31] and CMS [30, 33]. They are representatives for the evolution of silicon detectors in the last 3 decades. The numbers for the NA62 experiment are given for completeness. The power density of the readout chips increases with the number of readout channels per

detector. This has consequences on the cooling system.

From Delphi to BaBar, the power density of readout chips increased. During the last decade the readout chips for the CMS pixel detector benefited from developments in micro-technology, due to the commercial success of computers. Especially improvements in photolitography result in smaller feature sizes and therefore more integrated circuits per area. Smaller feature sizes can help to reduce the power consumption of a chip, while more circuits raise the power consumption, the power density and thus the heat dissipation. The readout chips for the NA62 GTK face another challenging peculiarity, the high trigger rate, which leads to high power density areas. In general the power density of future readout chips will rise, due to higher trigger rates in future trackers.

In addition to the rise of active silicon area and the rise in the power density of readout electronics, one can observe a drop in the target cooling temperature (radiation damage [50]). Subsequently the atmosphere in which the detectors operate had to be adapted to avoid condensation and additional heat input. In the future, the LHC experiments ATLAS, CMS and LHCb will cool their inner trackers with two-phase CO_2 circuits. Additionally LHCb will a use micro channel heat exchanger to cool the readout electronics in its CO_2 cooling circuit [68].

Table 2.1: Evolution of silicon detectors and their cooling

Experiment	Active Silicon	Detector Type	Power density	Cooling Fluid	Atmosphere	Cooling Technique
Delphi 1990 1997	$0.3\,m^2$ $1.6\,m^2$	strip strip/pixel	$0.17\,W/cm^2$ $0.56\,W/cm^2$	Water @ 20 °C	air at ambient temperature	cooling of support structure, conduction from readout electronics to cooling fluid, partly convection to ambient air
BaBar 1999	$0.96\,m^2$	strip/pixel	$1\,W/cm^2$	Water @ 8 °C	controlled, dry air at 8 °C	cooling of support structure, conduction from readout electronics to cooling fluid, partly convection to surrounding atmosphere
CMS 2008	$223\,m^2$	pixel	$0.2\,W/cm^2$	C_6F_{14} @-10 °C	controlled, dry nitrogen at -10 °C	cooling tubes under detector modules, connected to support structure, conduction from readout electronics to cooling fluid, partly convection to surrounding atmosphere
NA62 2014	$1.6E^{-3}\,m^2$	pixel	0.6 — 4 W/cm^2	C_6F_{14} @-20 °C	secondary beam vacuum, 10^{-6} mbar	silicon micro channels very close under the readout electronics, conduction to the cooling fluid

The Delphi MVD silicon vertex detector

In this detector design, the readout electronics could be placed on the left and right extremities of the Delphi Microvertex Detector (MVD). They did not overlap into the sensitive silicon cylinder. Figure 2.4 shows the complexity of the MVD. It was cooled via thermal conduction through the support structure holding the readout electronics. Water cooling lines were integrated into the support structure. Water at 20 °C kept the electronics from a thermal runaway. The temperature of the cooling lines and support structures was always above the dew point and no controlled atmosphere was needed. The power density of the readout electronics was $0.17\,\mathrm{W/cm^2}$ [34]. However, after the upgrade of the silicon tracker, the power density rose to $0.55\,\mathrm{W/cm^2}$ [77]. The heat flow had to pass several thermal connections between electronics and cooling water. This lead to temperature gradients between 4 °C and 12 °C. As a consequence, the detector had to run at higher temperatures. Higher temperatures also lead to more mechanical stress and deformation in the structures. As a further consequence, mechanical connections were broken and thermal connections were lost.

Figure 2.4: The Delphi VTX detector [81]

The BaBar SVT silicon vertex detector

The design of the BaBar silicon vertex detector is comparable to the Delphi's MVD detector, see Figure 2.5. The readout electronics are on the extremities of the detector and are cooled via conduction through the support structure.

Cooling lines were integrated in the structure. A difference is the temperature of the cooling liquid water. It enters with a temperature of 8 °C . This temperature is below the dew point temperature of a normal indoor atmosphere, which is around 11 °C . The detector had to be enclosed in a controlled atmosphere with dry air at 8 °C .

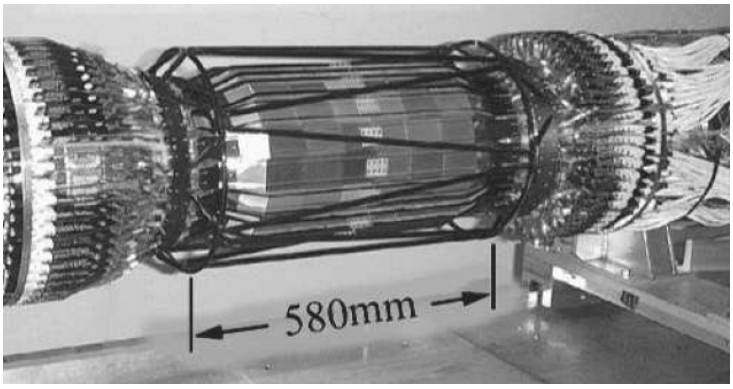


Figure 2.5: The BaBar SVT detector [31]

The CMS silicon tracking detector

The CMS and the ATLAS detectors are the largest of recent HEP detectors in collision experiments. The CMS inner tracker is state of the art technology and its installed active silicon surface is about 100 times larger than in the BaBar SVT. Figure 2.6 shows the size of the silicon strip tracker and the inner silicon pixel tracker of the CMS experiment. The collision energy in the CMS detector is very high, which leads to a high radiation environment. To avoid the rapid ageing of the tracking detector in operation it has to be cooled down to -10°Con the hottest point. Consequently the coolant is Perflourocarbon (C_6F_{14}),with a pour point of -90°C, and the detector needs to be in an controlled dry nitrogen atmosphere [30]. A water glycol mixture as cooling liquid would result in a to high pressure drop and it would be to dangerous in case of leaks.

The readout chips in the CMS pixel detector are located inside the detector volume, under the silicon pixel sensors and have a power density of $0.2\,W/cm^2$ [44]. This means that cooling lines run into the heart of the tracker to cool the readout chips. These cooling tubes run under the readout chips. In be-

tween tubes and chips are heat spreaders and pastes for good thermal contact. The temperature difference between the sensor and the coolant C_6F_{14} lies between 9 °C and 12 °C and between the readout chips and the coolant between 11 °C and 21 °C [33]. These high temperature differences lead to mechanical and displacement problems.

Before the Long Shutdown 2 (LS2), foreseen in 2019, the inner pixel detector needs to be replaced. The luminosity of the LHC and radiation level will rise significantly after LS2. This means that the tracker needs to run colder to avoid rapid ageing. A two-phase cooling circuit with CO_2 is foreseen to cool the tracker. The reduction of the temperature difference between chips and cooling fluid is important to avoid CTE (coefficient of thermal expansion) problems.

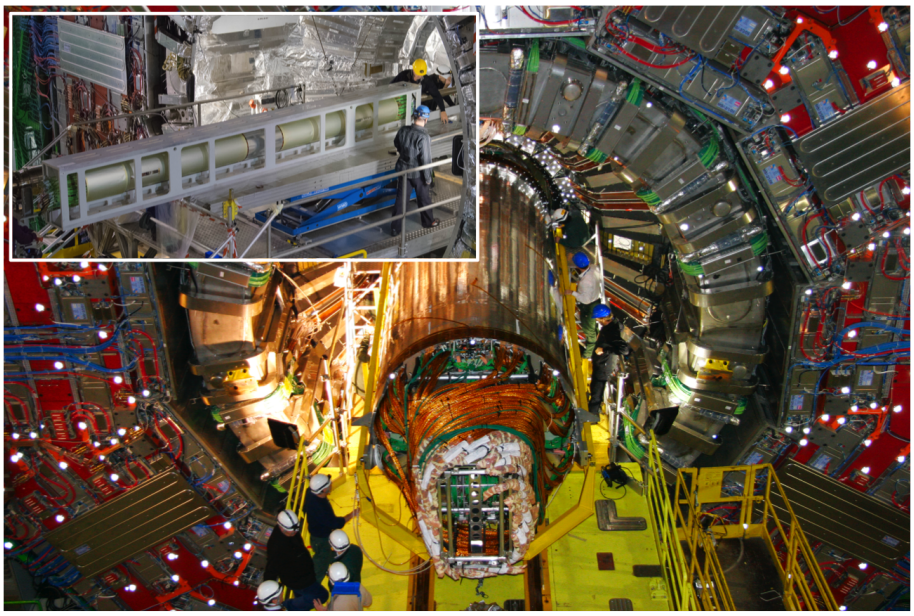


Figure 2.6: The CMS silicon strip tracker (large picture) and the CMS silicon pixel tracker (small picture) before the installation into the experiment. Courtesy of the CMS experiment

2.2.2 New Silicon Detector Cooling Challenges

Large and larger surfaces of silicon are involved and a total heating power of up to several tens of kW must be removed from tightly confined volumes for the coming generation of silicon detectors [30]. HEP tracking detectors have special operational constraints and some important parameters must be minimized in order to guarantee the required performance:

- The amount of material crossed by particles, because unwanted particle interaction with matter creates multiple scattering. The likelihood of particle-matter interaction rises with the material thickness.
- The temperature difference between heat source and heat sink for a given quantity of heat to be removed, because high temperature differences lead to high CTE mismatches. This can lead to mechanical stress, deformation and destruction.
- The temperature gradients on the surface of the sensor, because the pixel detector performance strongly depends on temperature uniformity.

Furthermore, the detector layout is often very packed and geometrically complex, thus only limited space is available for piping and connections. The thermal management of today's trackers is based on complex networks of mm-sized metallic pipes brought in connection with the heat sources through customized low mass heat spreaders [30]. Due to the small contact surfaces and the long chains of thermal resistances, today the temperature difference between the module surface and the coolant typically ranges between 15 °C and 25 °C for electronics power densities generally not exceeding $2\,W/cm^2$. In many cases, in order to preserve the silicon sensor from severe degradation caused by the high level of radiation, it is necessary to operate and maintain the detectors at temperatures in the range -10 °C to -20 °C [50]. With the above mentioned temperature differences, extremely low temperatures of the coolant are required. Moreover, this increases the problems of CTE mismatches between the silicon heat source and the heat sink, which needs to be specifically designed to deal with resulting large displacements and mechanical stresses in and between structural and active materials. Micro channel cooling in silicon wafers is a promising candidate to deal with the challenges mentioned above.

2.3 Micro Channels for HEP Detector Cooling

The big challenges listed in the previous section, 2.2.2, call for an innovation effort in detector cooling technology.

In 1981 Tuckerman and Pease [80] first described the use of silicon micro channel cooling for high power densities. Local thermal management through microfluidic heat sinks is in particular under study for the implementation in high power computing. Results with micro-fabricated heat sinks show their capability to remove heat up to $700\,\mathrm{W/m^2}$. Examples span from 2 mm thick silicon assemblies, designed for single phase water cooling, to thick copper plates, optimized for two-phase refrigerants [36, 51].

Although, the design of on-board cooling for HEP tracking detectors involves power densities which are in general two orders of magnitude lower [62], silicon micro channel cooling may actually provide a solution to the issues previously described. The principle idea can be seen in figure 2.7.

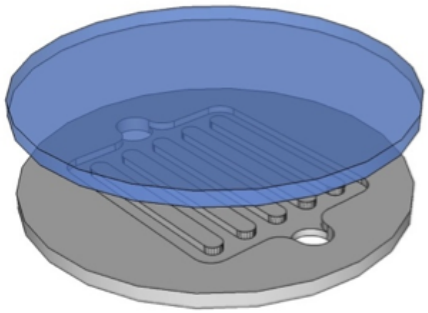


Figure 2.7: Schematic of a micro channel wafer and a closing wafer [59].

The idea relies on the use of standard MEMS technique to microfabricate in a thin silicon wafer a multi-channel hydraulic circuit with suited geometry. The channels are then closed by bonding a second wafer on the structured surface. The two wafers are then cut and thinned forming one or more cooling devices. The micro channel devices are then placed directly under the heat source, the readout electronics, see figure 2.8. Micro channel devices can be designed for single phase or two-phase flow. In the present study single phase cooling has been selected.

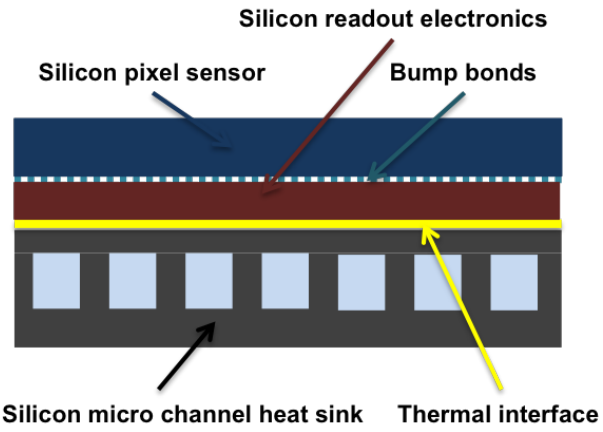


Figure 2.8: Principle of cooling with micro channels

2.3.1 Thermo-Hydraulic Layout of Micro Channels

The aim is to provide the significant dimensions of micro channels with single-phase coolants, to fulfil thermal and hydraulic constraints, which are height h, width w and spacing u between the middle of two channels. The length of the channels is given by the pixel sensor and the readout electronics, see Figure 1.5. The scheme in figure 2.9 shows the layout of the micro channels. They run in a straight line under the area, which has to be cooled. The coolant will enter and exit the channels via manifolds. These manifolds are integrated in the silicon micro channel heat sink. The width of the channels and the distance between them define the number of channels that can be placed under the electronics. The height of the channels is dictated by the physics requirements of the detector, namely the material budget allowed for cooling. Height, width and distance define the pressure drop for a given mass flow.

The following assumptions and constraints have been used for the optimization of the micro channel layout:

- The mass flow $\dot{m}$ in the micro channels is defined by the heat load $\dot{Q}$ that has to be removed from the readout chips and a reasonable temperature rise of the cooling liquid between inlet and outlet.
- The temperature difference of the coolant between inlet and outlet is

given and small, to obtain a relatively uniform temperature distribution and minimize thermal stress.

- The pressure drop is directly related to the mass flow, because the flow is laminar, due to the small dimensions of the channels; the law of Hagen-Pouisseulle (adapted for square shaped channels) can be applied.
- The spacing b between the middle of two channels varies between $3/2\,w$ and $2\,w$. The spacing b relates the width of the micro channel w to the width of the silicon wall w_w between the channels, $b = w + w_w$.
- The heat flux $\dot{Q}$ is evenly spread over the micro channel surface A and the average heat flux density is $\dot{q}$. Hot spots in the readout chips are levelled by the good heat conduction of the silicon.
- The hydraulic length and the thermodynamic length of the channels is $L = l$. The full length of the micro channels is used for heat exchange.

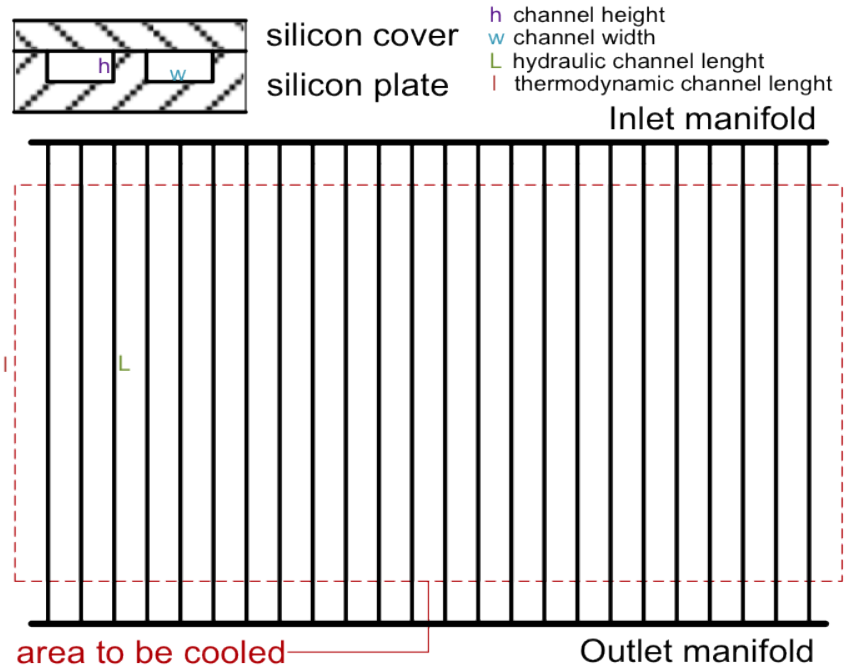


Figure 2.9: Micro channel layout with the important dimensions

The micro channel plate acts as a heat sink or heat exchanger to the readout electronics. The heat load affects the liquid running in the channels in two ways:

- a convective heat transfer, depending on the heat transfer coefficient h, the heat exchange surface A and the temperature difference ΔT between the fluid temperature T_f and channel wall temperature T_{wall}

$$\dot{Q} = hA(T_{wall} - T_f) \tag{2.4}$$

- a capacitive heat transfer, depending on the mass flow $\dot{m}$, the specific heat capacity c_p and the temperature difference ΔT between inlet and outlet

$$\dot{Q} = \dot{m}c_p(T_{out} - T_{in}). \tag{2.5}$$

As mentioned before one can assume that a liquid flow in micro channels is purely laminar and steady. This means the Hagen-Poisseuille formula [39]

$$\dot{V} = \frac{\pi D^4 \Delta p}{128 \nu \rho L} \tag{2.6}$$

can be used to calculate the pressure drop Δp inside the micro channels. In this formula $\dot{V}$ is the volumetric flow, D is the tube diameter, ν is the kinematic viscosity, ρ is the density and L is the length of the tube.

A first approach is to treat each channel as a single round channel with the heat load $\dot{Q}_C$, being the n^{th} fraction of the total heat load $\dot{Q}_{tot}$, with n as the number of channels. Let s be the length coordinate of a channel, with zero at the inlet and $s = L$ at the outlet. Assuming that Δp is a given pressure drop for one channel, this gives a thermal line load per channel of

$$\frac{d\dot{Q}_C}{ds} = b\frac{d\dot{Q}_{tot}}{dA_{HX}} \tag{2.7}$$

for a micro channel heat sink with the surface heat load $d\dot{Q}_{tot}/dA_{HX}$ and the spacing b between adjacent channels. The dimensionless Nusselt-number Nu relates the convective heat transfer to a fluid to the conductive heat transfer

inside a fluid [47]. For a round tube the characteristic length is the diameter D, h is the convective heat transfer coefficient and k is the thermal conductivity:

$$Nu = \frac{hD}{k} \tag{2.8}$$

Since the flow in micro channels can be assumed to be laminar, the Nusselt-number is a constant, [39]. In a fully developed laminar flow with a constant heat flux it can be calculated to

$$Nu = 4.364. \tag{2.9}$$

This means the line load per channel can be expressed using equation 2.4 and 2.8 as

$$\frac{d\dot{Q}_C}{ds} = \pi k Nu(T_{wall}(s) - T_f(s)). \tag{2.10}$$

It is important to mention that for this configuration with round channels, the heat flux is independent of the tube diameter D. To calculate the inner tube surface A, one uses D in the calculation of the perimeter (πD). The diameter D then also appears in substitution of the heat transfer coefficient h with the definition of the Nusselt-number from equation 2.8, which means D can be reduced.

In micro channels with rectangular cross section, one needs to introduce a factor C that relates the hydraulic perimeter, build with the hydraulic diameter D_H ($4A/P$), with the geometrical perimeter:

$$C = \frac{\pi D_H}{2w + 2h}\,. \tag{2.11}$$

Since the Nusselt-number equation also uses the hydraulic diameter, one can reduce the hydraulic diameter and the final equation for rectangular channels becomes easier to read

$$\frac{d\dot{Q}_C}{ds} = \frac{1}{C}\pi k Nu(T_{wall}(s) - T_f(s)). \tag{2.12}$$

Equation 2.10 describes the contribution of convection to the wall and fluid temperatures. To get a complete picture of the pressure drop and temperature differences necessary to transport the heat away, one also needs to look at the capacitive part of the heat transfer to the fluid, which means that the fluid heats up on its way through the micro channel. The fluid temperature along the channel can be expressed by the following equation

$$T_f(s) = \frac{1}{\dot{m} c_p} \int_0^s \frac{d\dot{Q}_C}{ds} ds \quad \text{with} \quad \dot{m} = \dot{V}\rho. \tag{2.13}$$

Combining equations 2.10, 2.6 and 2.13 gives an equation for the heat transfer along round micro channels

$$\frac{d\dot{Q}_C}{ds} = T_{wall}(s) \left(\frac{1}{\pi k Nu} + \frac{128 \nu L}{\pi c_p D^4 \Delta p} s \right)^{-1}. \tag{2.14}$$

Of particular note is the quadratic influence of the channel length L ($L \cdot s$) on the transferable heat. This means that the concept of micro channels becomes unfavourable for very long channels.

For micro channels with a rectangular cross section the Hagen-Poisseuille formula changes in the following way, [23]

$$\dot{V} = K_f(h,w) \cdot \frac{min(h,w)^3 \, max(h,w)}{12} \cdot \frac{\Delta p}{\nu \rho L}. \tag{2.15}$$

K_f is a correction factor that considers the geometric relation ship between the height h and the width w of the channel

$$K_f(h,w) = 1 - \sum_{i=1}^{\infty} \left[\frac{1}{(2i-1)^5} \cdot \frac{192}{\pi^5} \cdot \frac{min(h,w)}{max(h,w)} \cdot tanh\left[(2i-1) \cdot \frac{\pi}{2} \cdot \frac{max(h,w)}{min(h,w)} \right] \right]. \tag{2.16}$$

For the GTK micro channel dimensions (see 3.1) of h=70 µm w=200 µm one can calculate the correction factor to $K_f \approx 0.78$. Inserting 2.15 and 2.12 into 2.14

gives an equation that allows the calculation of the thermo-hydraulic behaviour of one micro channel along the flow direction,

$$\frac{d\dot{Q}_C}{ds} = T_{wall}(s) \left(\frac{1}{\pi k Nu}\, C + \frac{12\nu L}{c_p\, K_f(h,w)\, min(h,w)^3\, max(h,w)\, \Delta p} s \right)^{-1}. \tag{2.17}$$

Since the line load per channel ($d\dot{Q}_C/ds$) is normally fixed, due to the predicted heat dissipation of the readout electronics, it is more convenient in the design and evaluation period to look at the result of the line load, hence the temperature of the wall that encloses the channel. Equation 2.17 can be better interpreted when written in the following way

$$T_{wall}(s) = \frac{d\dot{Q}_C}{ds} \left(\frac{1}{\pi k Nu}\, C + \frac{12\nu L}{c_p\, K_f(h,w)\, min(h,w)^3\, max(h,w)\, \Delta p} s \right). \tag{2.18}$$

T_{wall} in equation 2.18 quantifies the offset that has to be added to the inlet temperature T_{inlet} of the coolant to describe the temperature behaviour of the bulk material that forms the channel along the flow direction. Due to the laminar nature of the flow in micro channels the convective heat transfer from the wall to the fluid results in a constant temperature offset independent of the channel length s. However, the capacitive heat transfer can be influenced via the choice of the coolant, the geometry of the channel and the allowable pressure drop.

One can assume that the choice of coolant has been taken and depends also on other HEP requirements and the pressure drop shall be kept low to minimize the material thickness on top and bottom of the channels. In this case, the temperature offset T_{wall} can be reduced, which means raising the mass flow $\dot{m}$, by optimising the height h and the width w of the channel and their ratio. One should pay particular attention to the fact that always the smaller of the two dimensions, h and w, influences T_{wall} and $\dot{m}$ with the third power. This means

for HEP applications, where the height of micro channels is usually limited by the available material budget (see 1.3), the ratio between channel width w and channel height h should not exceed 3/1. The gain in mass flow $\dot{m}$ becomes marginal if the ratio rises over this value. Figure 2.10 is an example from the calculations done for the GTK micro channel heat sink that illustrates this effect. It shows the mass flow $\dot{m}$, that can be reached with varying the channel width w. The channel height h is fixed to 90 µm , the available pressure drop Δp is fixed to 2 bar and the spacing between channels is fixed to $b = 3/2\,w$. A channel width greater than three times the channel height results only in a small mass flow rise.

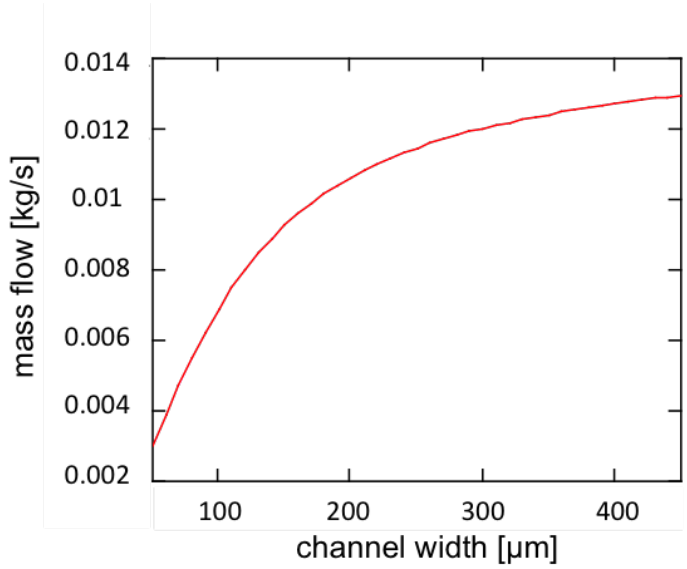


Figure 2.10: Mass flow rate of C_6F_{14} over channel width w for the GTK micro channel heat sink ($h = 90\,\mu m$, $\Delta p = 2\,bar$, $b = 3/2\,w$)

2.3.2 Hydraulic Layout of Channels and Manifolds

As described in 2.3.1, an analytical approach can be used for the thermo-hydraulic layout and subsequently the hydraulic layout of micro channels. The pressure drop and the mass flow rate can be calculated. Numerical simulation is used to verify the results.

For a complete hydraulic layout of the micro channel heat sink one needs to include the manifolds into the layout process, since they contribute to the overall pressure drop. The manifolds connect the individual channels at their inlet and outlet, see figure 2.7. They distribute and recollect the coolant. The manifolds are connected to the piping of a fluid circuit via through holes. An analytical calculation of the hydraulic pressure drop inside the manifolds is not possible, since the flow regime can change inside them from turbulent to laminar.

An approximation to quantify the pressure loss that occurs in the manifolds is to assume that the kinetic energy of the flowing liquid is lost when entering from the tube into the manifold. It gives an order of magnitude of the manifolds pressure loss. As the system has an inlet and an outlet manifold the pressure loss can be estimated to

$$\Delta p_{manifold} = 2 \cdot \Delta p_{kin} = 2 \cdot \frac{\rho}{2} v_{in}^2. \tag{2.19}$$

Herein ρ is the density of the fluid and v is its velocity at the inlet of the manifold. The real flow conditions and geometric conditions are not taken into account by this method. Therefore one can only use it as a first approximation when starting the layout process. Additionally this method cannot predict the distribution of the coolant into the parallel micro channels.

A more sophisticated method to study the flow conditions, the pressure drop and the flow distribution inside the micro channels and its manifolds is to create a 3D-model of the micro channel geometry, see figure 2.11, and use Computational Fluid Dynamics (CFD) for predictions. CFD uses the Reynolds-averaged Navier-Stokes equations to describe fluid phenomena [46]. The fluid volume is divided into cells that form a mesh. Boundary conditions are defined on the enclosing surfaces. The equations for each cell are then solved iteratively. A post processor visualizes the results, see figure 2.13. In this case the commercial software Ansys CFX was used to simulate the flow.

Figure 2.11 shows a first prototype of a micro channel heat sink. The inlet and outlet holes are located centrally on top and bottom of the micro channel area and connect the piping to the manifolds. The channel cross section in this case is 100 µm × 100 µm . The micro channel silicon wafer is in this case bonded to

a pyrex wafer to close the fluid circuit. The micro channel and manifold design is a first trial and used to prove the concept. The wafer was tested in the C_6F_{14} test stand. The CFD model on the right of figure 2.11 only represents half of the real heat sink geometry, since it is symmetric to the plane that goes through the center of inlet and outlet.

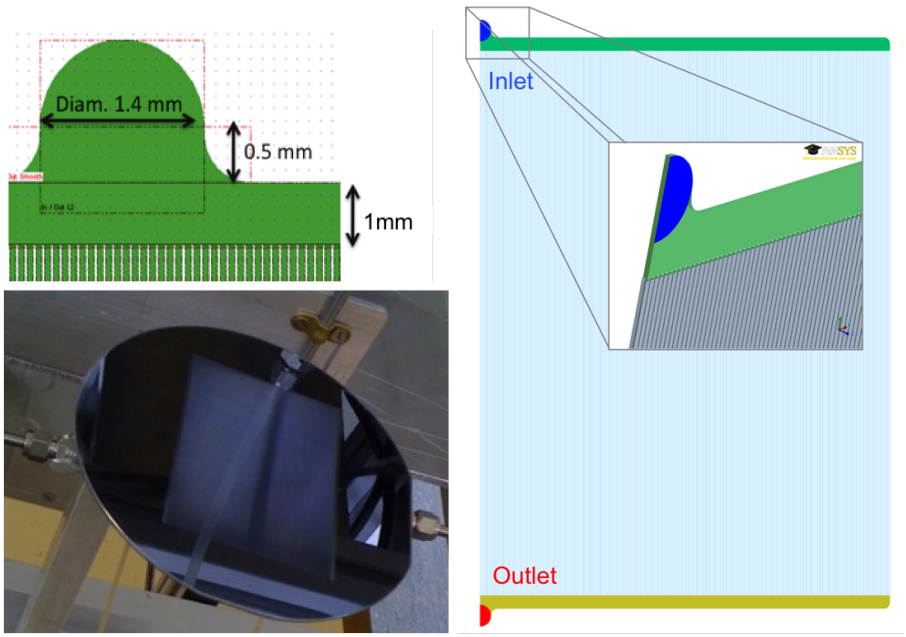


Figure 2.11: First micro channel prototype with central inlet and outlet in hydraulic test; belonging CFD half model.

Figure 2.12 compares the simulated pressure drop with the values measured with the first prototype heat sink wafer. The chart shows a very good agreement between the simulated and the measured values. This means that for further design optimizations one can use the CFD to predict the the total pressure drop.

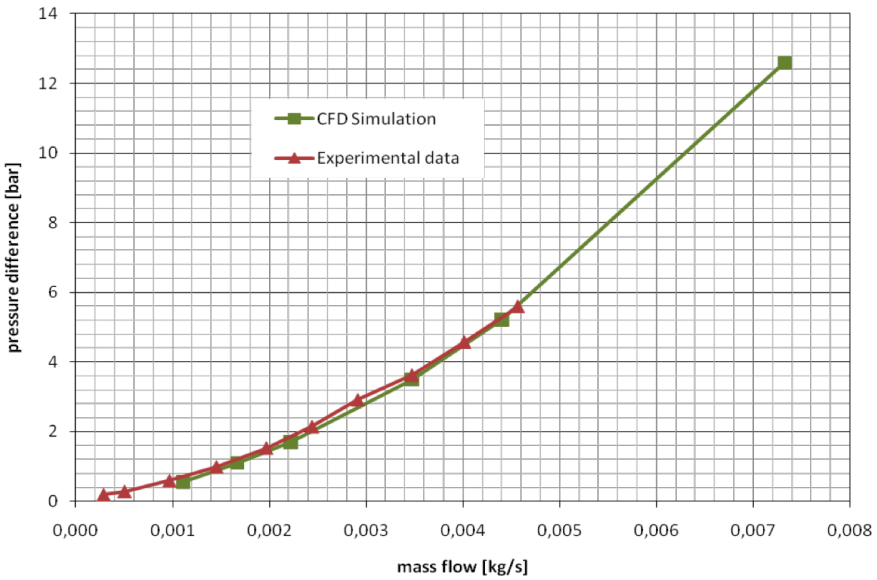


Figure 2.12: Comparison of the measured and the simulated pressure drop of the first prototype.

The flow distribution inside the micro channels and manifolds can also be predicted with CFD. The velocity chart on the right side of figure 2.13 indicates that in this very first prototype most of the mass flow will go through the micro channels placed in the center. The micro channels further away from inlet and outlet see less flow velocity, hence mass flow rate. A simple test setup with a kapton heater and a thermal camera is shown on the left side of figure 2.13. The thermal pictures qualitatively prove the preference of the coolant to flow through the middle of the micro channel array. Since these tests have to be done in normal atmosphere, the coolant temperature was kept above the dew point to avoid condensation.

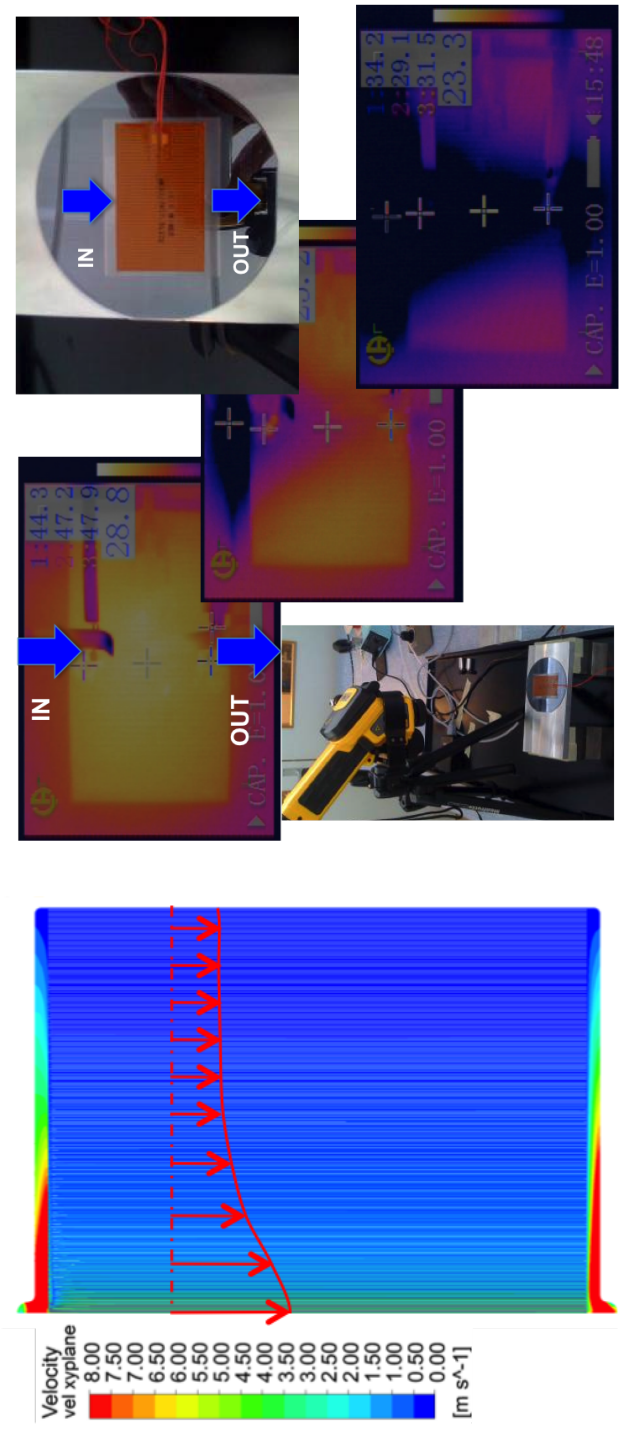


Figure 2.13: Verification of the flow distribution of the first prototype. CFD prediction of the velocity distribution (left) and IR images of the temperature distribution under uniform surface heat load (right). The mass flow pattern predicted by the CFD model could be confirmed.

3 Micro Channel Cooling for the NA62 GTK

Micro channel (mc) cooling was chosen as the baseline cooling solution for the NA62 GigaTracKer in October 2012. This chapter explains how the thermo-hydraulic layout of channels and manifolds was realized for the GTK. It also describes the production process of the micro channels and the test set-up which was used to test the micro channel cooling plate and the alternative micro channel cooling frame.

Cooling Fluid C_6F_{14}

C_6F_{14} was selected as the coolant for the GTK. The following features led to its choice [45]:

- radiation hard,
- thermally and chemically stable,
- non-flammable, non-toxic, dielectric,
- known and used at CERN (CMS and Atlas Tracker),
- allows cooling in liquid phase below 0°C.

Table 3.3 shows its most important thermo-hydraulic properties in comparison to water. Although water is thermodynamically the better liquid phase coolant, C_6F_{14} will be used for the above mentioned reasons.

Table 3.1: Properties of the coolant C_6F_{14} [14] compared to Water [3]

Property	C_6F_{14} @ -25°C	H_2O @ 20°C
Density $\rho\,[\frac{kg}{m^3}]$	1805	998
Viscosity $\nu\,[10^7\frac{m^2}{s}]$	8.2	10
Heat capacity $c_p\,[\frac{J}{kg\ K}]$	975	4183
Thermal conductivity $\lambda\,[10^{-2}\frac{W}{m\ K}]$	6.275	60

3.1 Baseline Design for the Heat Sink - Cooling Plate

The considerations and techniques described in 2.3.1 and 2.3.2 were used to optimize the thermal-hydraulic layout of the baseline design of the GTK silicon heat sink. The baseline design of the heat sink consists of parallel micro channels, manifolds connecting them and inlet/outlet holes. The micro channel designs were developed in the frame work of the CERN PH-DT cooling group by a collaboration between the CERN PH-DT group, the CERN PH-ESE group and the UCL CP3 institute [59]. The structures are engraved into a silicon wafer and closed with another silicon wafer by silicon fusion bonding or with a transparent Pyrex wafer by anodic bonding. The micro channel heat sinks were produced in EPFL CMi cleanroom [54, 1]. The resulting object is also called a cooling plate. The final design of the channels was predominantly influenced by the material budget allowed in the sensitive area of the detector and the constraints in the production process, especially the bonding between the two wafers.

Micro Channel Dimensions

The material budget limited the cooling plate to a maximum thickness of 150 µm[27] in the sensitive area. It was decided to keep the maximum height of the channels to 70 µm. This leaves a total thickness of 40 µm silicon above

and below the micro channels in the sensitive area. If necessary for the physics measurements, this thickness can be reduced to 30 µm, which would result in a total thickness of 130 µm. Figure 3.1 shows a schematic cross section of the micro channel cooling plate. One can see the two areas that have to be thinned for physics performance. The difference in size is due to the fact that the upper part will host the sensor assembly, 10 readout chips bump bonded to the silicon pixel sensor, and the lower part only needs to be thinned in the sensitive area. The manifolds can be of different depth, since they are placed outside of the sensitive area.

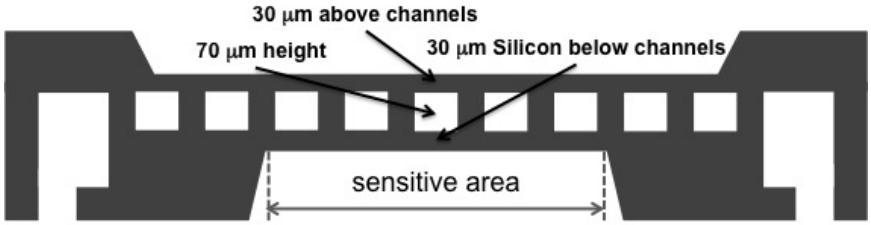


Figure 3.1: Schematic cross section of the baseline design

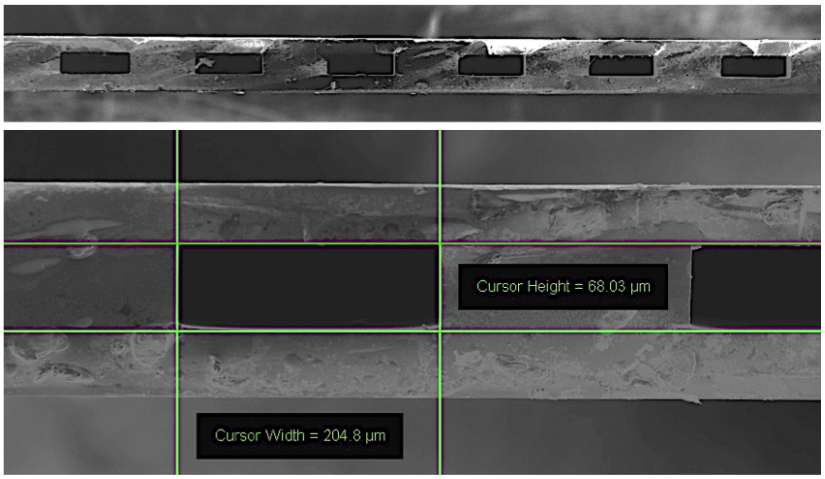


Figure 3.2: Magnification of a cross section cut through a baseline cooling plate, the silicon wafer with channels is fusion bonded to a silicon cover wafer. Courtesy of CSEM

To keep the pressure drop in the channels low, the channel width was fixed to 200 µm. Consistently with the statement from 2.3.1, the width is less than 3 times bigger than the height of a channel. The nominal mass flow is the mass flow necessary to remove the expected heat load and is a result of equation 2.5. The spacing between 2 channels is fixed to 400 µmfor production reasons, which results in a wall width between two channels of 200 µm, see figure 3.2. This leaves enough material between the channels to guarantee a good fusion bonding between the 2 silicon wafers [82]. The expected pressure drop caused only by the micro channels in this configuration at nominal mass flow is around 2 bar, see table 3.2.

A smaller spacing would be desirable to raise the total channel cross section for the coolant flow, resulting in a higher mass flow rate or smaller pressure drop. Trials with Pyrex glass wafers as cover wafers showed that channel walls down to 20 µm are feasible without the risk of weakening the structure, see figure 3.3. However, the bonding of 2 silicon wafers via fusion bonding needs more surface between channels to perform a reliable bonding. In future heat sinks, the bonding performance might improve and the wall thickness could be reduced.

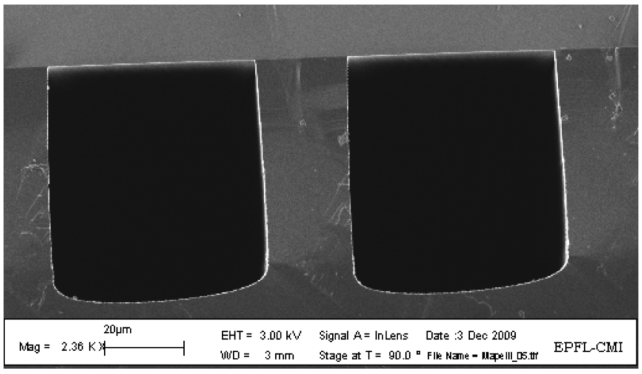


Figure 3.3: Magnification of a cross section cut through a cooling plate with 20 µm channel walls. The silicon wafer with channels is bonded to a Pyrex cover wafer. Courtesy of EPFL CMi

Manifold Dimensions

To feed the micro channel cooling plate with its coolant, C_6F_{14}, Nanoport® connectors from Upchurch Scientific have been chosen in the test phase. Nanoport® connectors are commercially available fluid connections for chip-based applications and analyses [9]. They connect to bendable peek tubes, which allows easy adaptation when the test setup changes. In the final installation one needs a more rigid and non detachable connection solution. A good candidate is the chip-to-tube soldering described in subsection 5.2.1. The first part of the Nanoport® is glued to the surface of a micro channel wafer, covering the inlet/outlet hole, and the second part is connected to a peek tube and can be screwed into the first part. The peek tube is then connected to standard stainless steel piping in the test stand. The inlet/outlet holes in the wafer have a diameter of 1.6 mm, which corresponds to the inner diameter of the Nanoport® connectors. This avoids unwanted restriction of the flow. For this connection solution the manifold to distribute the coolant to every channel has to be embedded into the cooling plate. The thickness of a standard silicon wafer (525 µm) limits the depth of the manifold. The mechanical stability limits the maximum width of the manifold. The standard width of the manifold was set to the size of the connecting hole, 1.6 mm.

Since the dimensions of the channels must take into account other than thermal-hydraulic constraints, it is important to improve the hydraulic performance of the manifolds inside the silicon cooling plate. The results from the first prototype, see figures 2.12 and 2.13, show the flow maldistribution in the channel area and the high pressure drop inside the manifolds. However, the principle of cooling with silicon micro channels was proven.

To improve the flow distribution over the channel area, the inlet and outlet holes have to be placed on opposite sides of the channel area, see figure 3.5 . This guarantees that the length of the flow path between inlet and outlet through a micro channel heat sink is constant, independent of the channel it goes through [85, 79]. The result is an equal pressure drop of flow paths going through the first, the last or any other channel in between. Consequently the coolant distributes itself evenly over the channel area and every channel is fed with the same mass flow, resulting in an equal cooling performance per channel.

The pressure drop inside the micro channels is fixed by their geometry, the

mass flow that is necessary to carry away the heat load and the flow regime, namely laminar flow. A further reduction of the total pressure drop inside the micro channel cooling plate can only be reached inside the manifolds. Herein an important decision in the design process was to allow more material outside of the sensitive area, which consists of the size of the silicon pixel sensor plus a 10 mm safety area around it, see figure 1.5. This allows to make the manifolds deeper and to reduce the total pressure drop of the micro channel cooling plate significantly. The simulation results in Figure 3.4 show the significant effect of the manifold depth on the total pressure drop, especially when running higher mass flows.

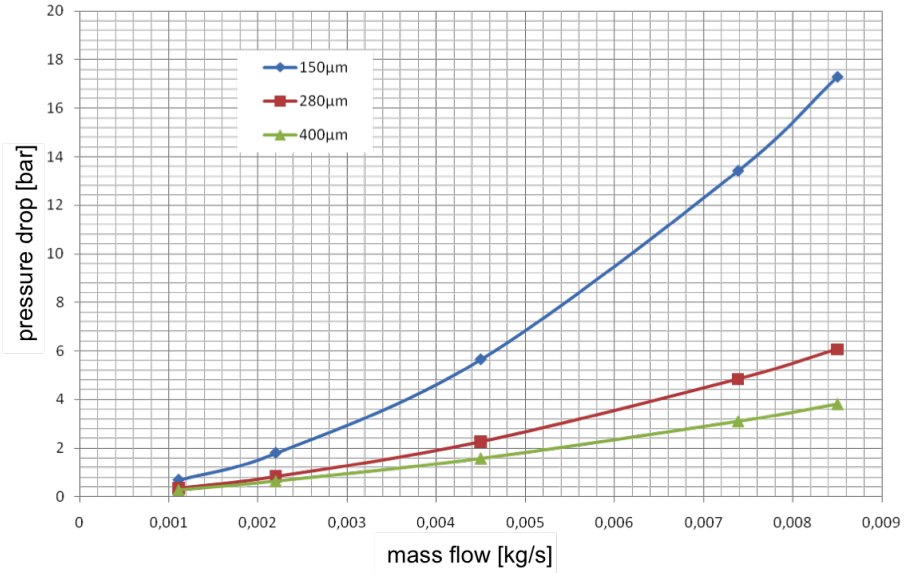


Figure 3.4: Simulated total pressure drop over the mass flow. Manifold depth has a big influence on total pressure drop.

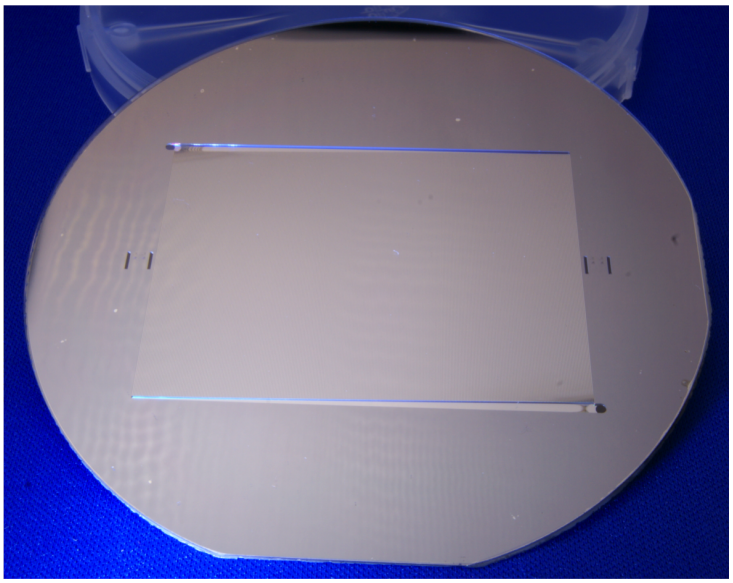
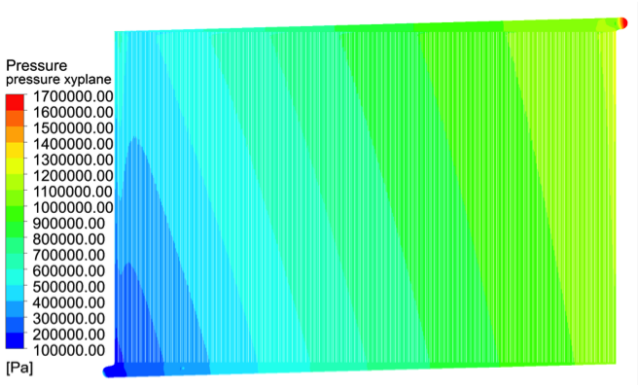
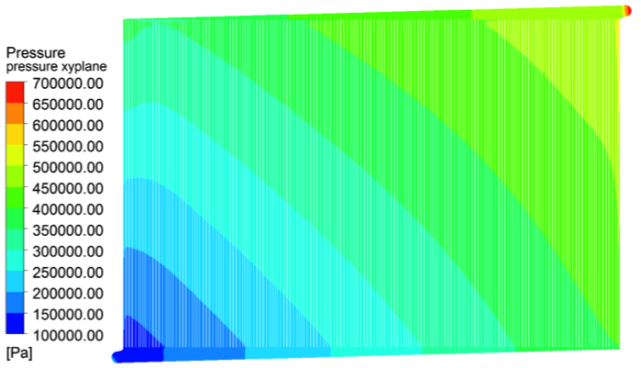


Figure 3.5: Silicon micro channel wafer with pyrex cover, deep manifolds and inlet/outlet diagonally opposite to each other

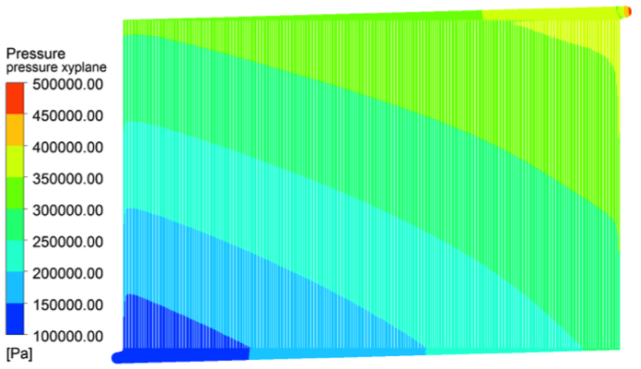
Figure 3.5 shows a silicon micro channel wafer, where the manifolds are deeper than the channels, and inlet/outlet holes are diagonally opposite to each other. The cover wafer in this case is a pyrex wafer, which allows faster production and visualisation of the flow. The design of this wafer had been tested and fulfilled the cooling requirements at that stage of the development. However, the final baseline design selected for the experiment is the result of a further optimization step to a lower pressure drop and is adapted to silicon-silicon fusion bonding.



(a) 150 µm



(b) 280 µm



(c) 400 µm

Figure 3.6: Pressure drop distribution on a xy-plane inside the micro channels for 3 manifold depths. The graphs correspond to the most right points of the graph in figure 3.4.

Figure 3.6 shows the pressure drop distribution at the nominal mass flow for manifold depths of 150 µm, 280 µm and 400 µm. The graphs 3.6a, 3.6b and 3.6c show the pressure drop distribution at the most right point of the corresponding manifold depth curve in the total pressure drop plot in figure 3.4. The channel geometry is the same in each case. First one sees the reduction in total pressure drop from 16 bar at 150 µm to 6 bar at 280 µm and to 4 bar at 400 µm. Secondly one can observe that the isobar lines become more horizontal with deeper manifolds. It indicates, that deeper manifolds generate less pressure drop. The reduction in total pressure drop is important for the mechanical stability of the micro channel cooling plate. Since the manifolds are much wider then channels, the pressure inside them acts on a much larger silicon membrane above and below. Consequently the silicon membrane close to the inlet hole is the weakest point, concerning a rupture caused by pressure.

Table 3.2 lists the different channel geometry and manifold geometry configurations that have been simulated for the baseline micro channel cooling plate. It also shows that a split of the flow into two inlets before the cooling plate significantly reduces the total pressure drop. It means that the cooled area is split into two parallel circuits with their own inlet and outlet manifold. Instead of 2 connectors, then the cooling plate has 4 connectors, which could rise the failure probability. Nevertheless, is a solution with 2 inlets and 2 outlets a good possibility to lower the total pressure at the inlets, where one finds the mechanically weakest point. The term half model in table 3.2 describes that only half of the channel area had been modelled. It means the modelled channel area is only 30 mm $\times$ 40 mm instead of 60 mm $\times$ 40 mm, which is the size of the channel area in reality.

Table 3.2: CFD simulations for the baseline micro channel cooling plate.

channel size		pressure drop channels		manifold size			pressure drop total	comments
height x width µm x µm	wall width µm	simulation Δp [bar]	analytical Δp [bar]	shape	width mm	depth µm	simulation Δp [bar]	
50 x 50	25	13	13,8	triangular	2	50	30	half model
					4	50	27	half model
				straight	2	50	30	half model
50 x 100	25	7	7	triangular	2	200	9,5	half model
						400	8	half model
100 x 100	25	1,50	1,44	straight	1	100	15	half model
				triangular	1,6	150	13,4	full model
						280	4,8	full model
						400	3,1	full model
				triangular	1,6	400	2,1	half model, 2 inlets, 2 outlets
100 x 100	100	2,4	2,3	triangular	1,6	280	5,6	full model
100 x 200	200	1,49	1,41	triangular	1,6	280	4,8	full model
90 x 150	75	1,65	1,60	triangular	1,60	400	2,2	half model
					1,60	400	2,1	half model, outlet 1.8mm width
					1,60	280	2,4	half model, outlet 2.1mm width

Baseline Dimensions

Double inlet/outlet holes/manifolds have been included in the design. The pressure drop inside the manifolds was drastically reduced, so that they act like a pressurized reservoir for the coolant. In this case a straight shape of the manifold provides a more constant pressure at the inlet of each micro channel. Figure 3.7 shows a cooling plate with the baseline design. The above mentioned criteria have been included in this design. The inlets and outlets had to be placed more outside of the channel area, to comply with the physics requirements, due to the size of the connectors. Hence, the manifolds have to bend outside as well. The backside of the cooling plate shows an impression that has been etched into the cooling plate. It has the dimensions to host the sensor assembly (pixel sensor with 10 bump bonded readout chips) or the thermal mock-up (3.4.1). The remaining silicon layer above the channels is 30 µm thick. Figure 3.8 shows a baseline cooling plate a with thermal mock-up as a schematic cross section and in reality, ready to be tested.

Table 3.3: Dimensions and features of the baseline micro channel cooling plate.

micro channels	height h	70 µm
	width w	200 µm
	wall width w_w	200 µm
	length l	42 mm
manifolds	shape	straight
	depth	280 µm
	width	1.6 mm
	length	34 mm
cooling plate	thickness inside sensitive area	130 µm
	thickness outside sensitive area	$\sim$ 500 µm
	connector	chip-to-tube soldering (5.2.1)

Figure 3.7: Baseline cooling plate with double inlet/outlet, backside with impression to host the readout chips/dummy electronics.

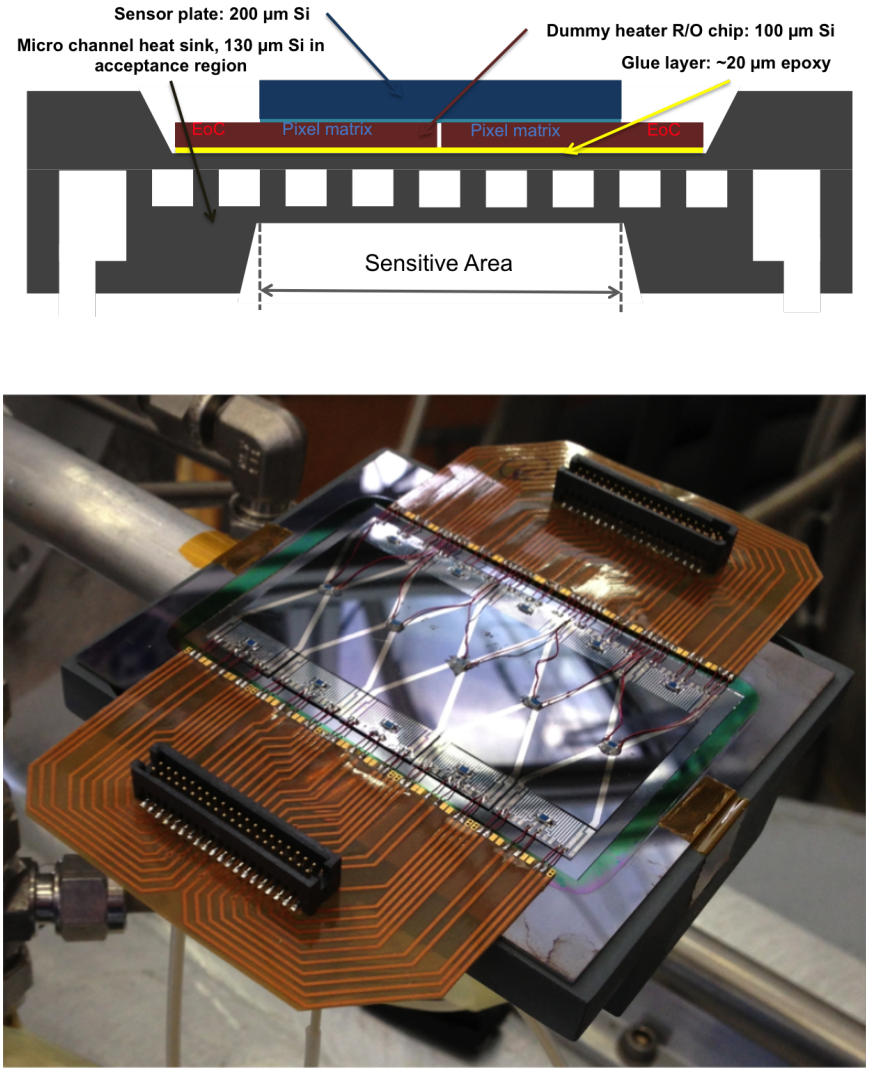


Figure 3.8: Schematic of the baseline cooling plate with a thermal mock-up (top) and a real baseline cooling plate with double inlet/outlet, equipped with a thermal mock-up (bottom).

3.2 Alternative Design for the Heat Sink - Cooling Frame

The readout electronics are the main heat source in the GTK-subdetector. Therefore it is important to know how the heat production is distributed over the area of one readout chip. With the decision to go further with the development of the TDCpix in an end-of-column (EoC) design, it became clear that the heat distribution will not be uniform over its surface. With the previously assumed configuration the heat distribution was expected to be evenly spread over the readout chip.

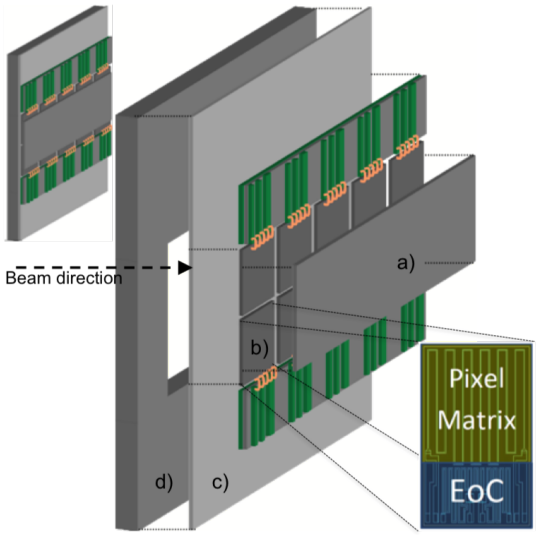


Figure 3.9: Schematic of the GTK subdetector and its readout chip TDCpix.

Figure 3.9 shows a schematic of the readout chip and its position inside the GTK subdetector. 10 readout chips process the data from the pixel sensor. The TDCpix [17] is an ASIC which can be divided into 2 sections. The pixel matrix contains the bump bonding pads and the analogue lines that transmit signals from the pixels to the End-of-Column region. The EoC region contains the digital logic that processes the signals. The EoC region will produce most of the heat. The results of the cooling tests in chapter 4 refer to the pixel matrix as "analogue region" and the EoC region as "digital region" for simplicity. This

naming convention does not entirely reflect the functionality of the region. Figure 3.10 shows the power estimations of the TDCpix in 2012.

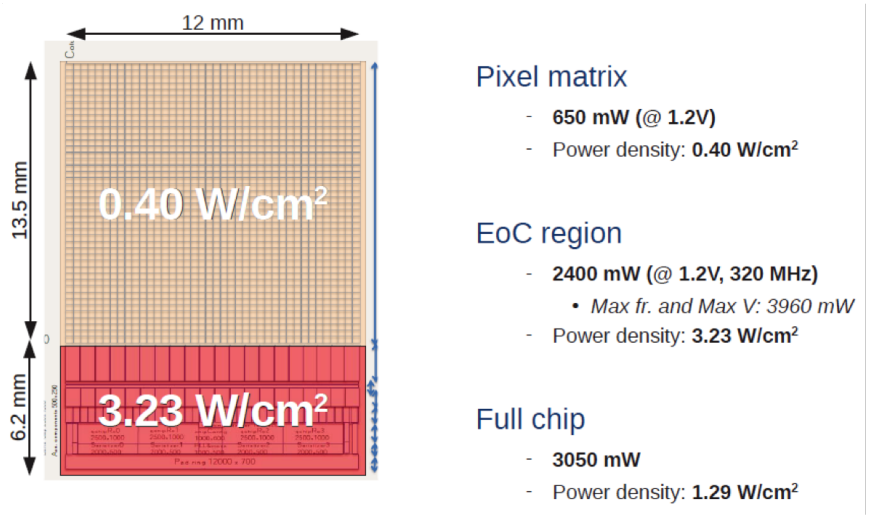


Figure 3.10: Estimated power dissipation of the TDCpix readout chip [67]

The preconditions mentioned above allowed the development of an alternative heat sink, where only the EoC region is cooled by micro channels, referred to as the "frame". Figure 3.11 shows the concept of the cooling frame. The sensitive area (pixel sensor) is kept free of additional material for cooling. The small amount of heat produced in the pixel matrix of the TDCpix is removed by conduction through the bulk silicon of the TDCpix. Figure 3.12 shows a cross section of the cooling frame with readout electronics in real dimensions. In the magnification one can see that the micro channels only run under the EoC region of the TDCpix.

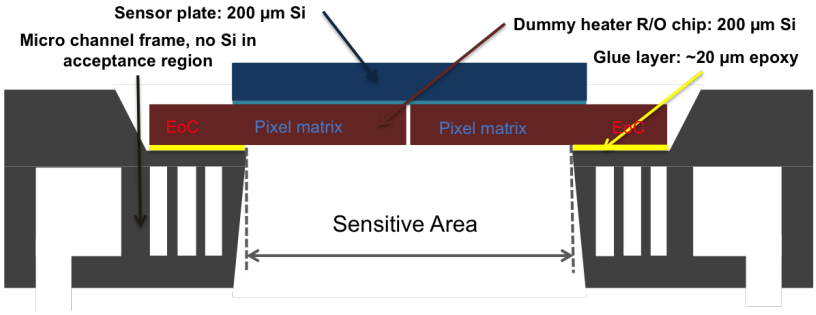


Figure 3.11: Schematic of the cooling frame with electronics.

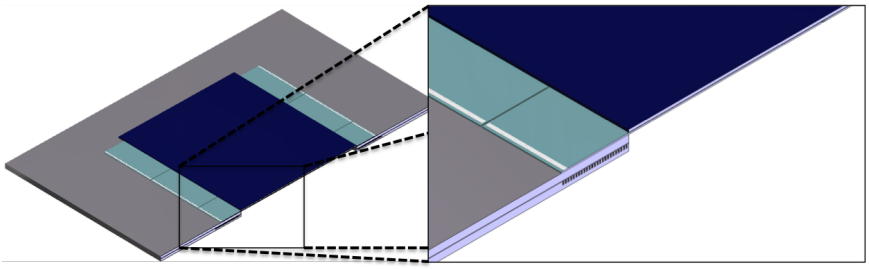
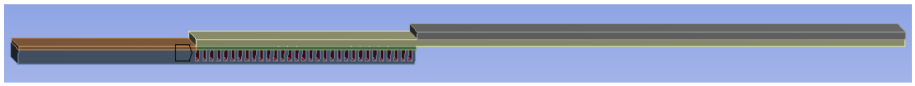
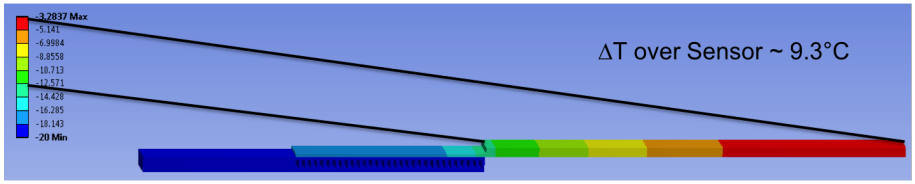


Figure 3.12: Cross section of the cooling frame in real dimensions. Enlargement of EoC region with micro channels running underneath.

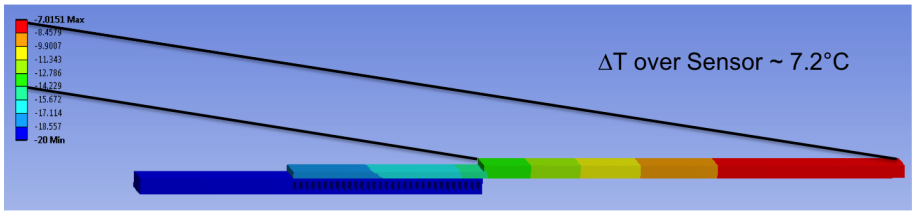
The physics requirements for the thickness of the TDCpix can and should be relaxed, if cooled via the frame. The TDCpix should be 200 µm thick, if cooled via the frame, in contrast to the 100 µm thickness allowed for a cooling plate. The doubling of the cross section of the TDCpix facilitates the conduction of the heat from the pixel matrix to the EoC region. Figure 3.13 illustrates this effect. The heat conduction problem in the middle of the cooling frame can be seen as a two-dimensional problem. Only a slice of the geometry has been modelled, figure 3.13a. A 100 µm thick TDCpix, figure 3.13b, has a higher temperature and larger temperature spread on its surface than a 200 µm thick TDCpix, figure 3.13c.



(a) Geometry



(b) TDCpix 100 µm thick



(c) TDCpix 200 µm thick

Figure 3.13: Simulation of temperature distribution in a GTK detector mounted on a cooling frame. The wall temperature of the channels is fixed to -20 °C .

Also the channel geometry has to be optimized for the cooling of the readout chips via the micro channel frame. The heat produced by the readout chips has to be drained via a much smaller surface (EoC region) to the coolant inside the micro channels. The inner surface of the micro channels needs to be enlarged, because the heat has to pass through it on its way to the cooling liquid. Otherwise the temperature difference, resulting from the convective heat transfer, between silicon and coolant becomes too large, which results in higher thermal stress. This temperature is also called junction temperature ΔT_j. The junction temperature is the driving force of the heat flux from the wall to the coolant. The junction temperature can be calculated following equation 2.4

$$\Delta T_j = \frac{1}{\pi \, \lambda \, Nu} \, \dot{Q} \, C \, . \tag{3.1}$$

The factor C, the ratio between hydraulic and geometric perimeter, corrects for square shaped channels. For a constant heat flux over the length of a channel,

the junction temperature is constant as well. Since the micro channels run only under the EoC region one can assume the heat flux to be constant. Figure 3.14 shows where the junction temperature jump appears.

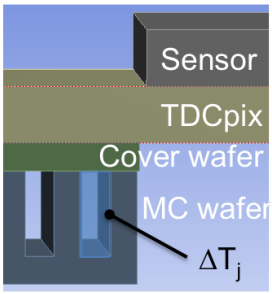


Figure 3.14: Enlarged slice of EoC region to illustrate where ΔT_j appears.

The achieved junction temperature has to be balanced with the allowed pressure drop that occurs in the micro channels, when the coolant flows through them. The graphs in figure 3.17 illustrate how the channel geometry influences the pressure and the junction temperature. Desirable values for both pressure and junction temperature, are marked in the graphs with a red rectangle. The area in which the channels run is fixed by the size of the EoC region. The minimum channel length is 60 mm (5 chips with 12 mm width) and in width the channels are bounded to 6.2 mm, the length of the EoC region. In general these graphs show that the channels should be narrow and deep. The comparison between the graphs 3.17a, 3.17b and 3.17c highlights the strong influence of the wall thickness between the channels. The thicker the wall, the less channels one can integrate into the 6.2 mm length of the EoC region. The results in figure 3.17c are the lowest and show that a wall thickness of 50 µm or less is necessary to effectively cool the EoC region.

The calculations were done under the assumption of a constant mass flow and a constant heat flux to the inner channel surface. The assumption of a homogeneous bulk silicon temperature is valid, if one looks at the high value for the thermal conductivity of silicon, 124 W/mK [3]. The simulations shown in figure 3.13 support the assumption that the temperature gradient inside the silicon cooling device is minimal.

Following the results shown in 3.17, the channels in the alternative frame heat

sink are 100 µm wide, 300 µm deep and have a pitch of 150 µm , which translates in 50 µm wide walls between channels. The channels are 60 mm long and the inlet/oulet manifolds add 5 mm on each side. For a more efficient production, the micro channels are produced as a stave and are later assembled to form a frame. Figure 3.15 shows a wafer with 4 micro channel staves and the inlet/outlet geometry. In the next step, the wafer is diced. 2 micro channel staves and 2 connecting silicon pieces are then glued together to form the frame. Figure 3.16 shows a micro channel frame with a silicon mock-up glued on top. Nanoport connectors are glued on top of the inlet/outlet holes of the manifolds. They ensure the connection of the test stand tubing to the micro channel cooling frame.

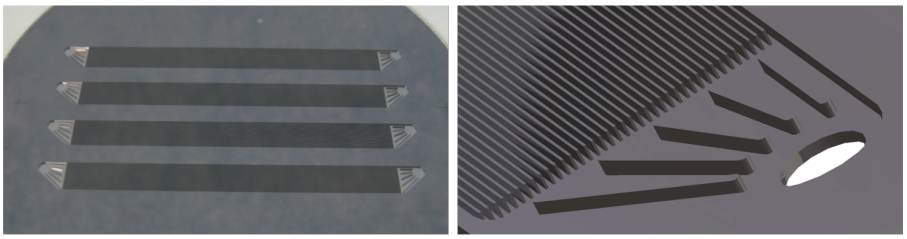


Figure 3.15: Wafer with 4 mc staves in an intermediate production step. 3D drawing of the inlet/outlet region.

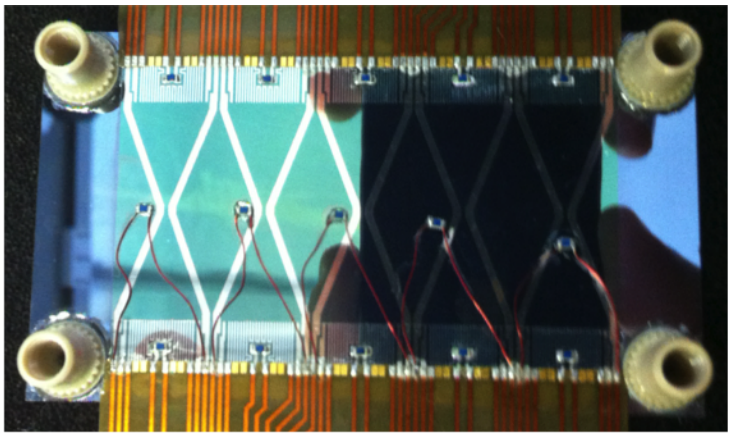
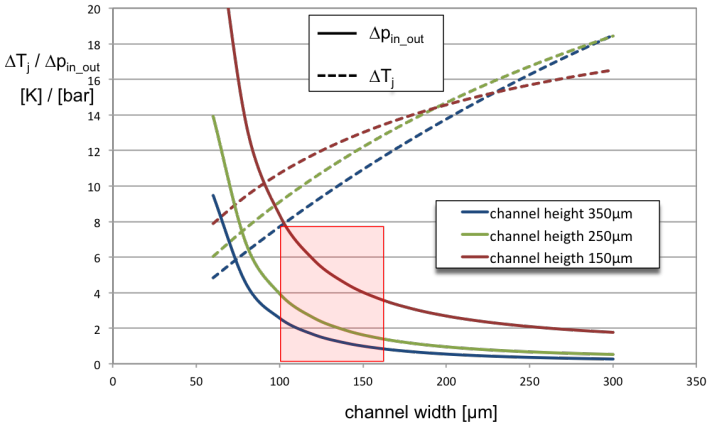
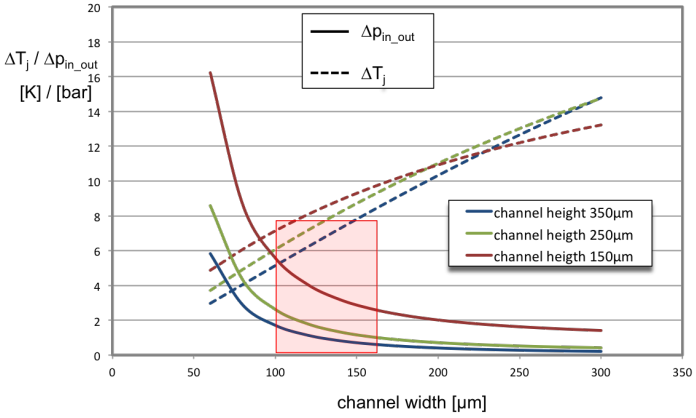


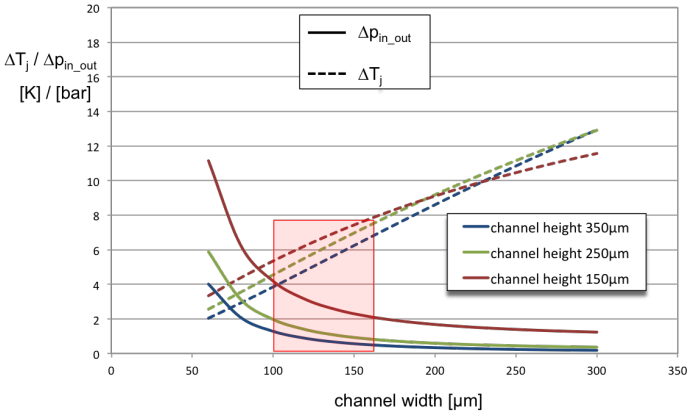
Figure 3.16: Micro channel frame with inlet/outlet connectors and silicon mock-up glued on top. The coolant runs horizontal from left to right or vice versa under the EoC region.



(a) wall thickness 200 µm



(b) wall thickness 100 µm



(c) wall thickness 50 µm

Figure 3.17: Analytical calculation on how the channel geometry influences the pressure drop and the junction temperature.

3.3 Micro Channel Production

The production of a micro channel heat sink uses several techniques, traditionally used in the semiconductor industry to produce electronic devices. Since the invention of the transistor in 1947, these techniques have been constantly subject to development and refinement. Today, the production process of silicon based semiconductors has reached the industrial level. Based on these micro-fabrication technologies, a new branch of products has been developed in the last years, namely micro electro-mechanical systems (MEMS). Microfluidic devices are a derivative of MEMS, which started with the development of lab-on-chip devices for chemical and biological tests [62].

The prototype micro channel heat sinks for the GTK subdetector (baseline and frame) are produced at the EPFL CMi (Center of MicroNanoTechnology) in Lausanne in collaboration with the Microsystems Laboratory [1]. The following basic techniques are used in the production of a micro channel heat sink:

- Photo-lithography; mask production and spin coating of photo-resists
- Etching; DRIE (Deep Reactive Ion Etching) and wet etching
- Thinning; mechanical grinding and chemical mechanical polishing (CMP)
- Bonding; direct silicon wafer (or fusion) bonding and anodic bonding for silicon and Pyrex wafers

Figure 3.18 shows a simplified production process of a micro channel heat sink. From step 3.18a to 3.18b the pattern from the photo-lithography mask is transferred to a silicon wafer, 4" in diameter and 380 µm or 512 µm in thickness. The wafer had been spin coated with a light sensitive resist, and after the light exposure through the mask, the unexposed resist can be washed out. The remaining resist protects the silicon underneath during the etching in step 3.18c. One distinguishes between DRIE etching with a plasma and wet etching in a chemically attacking solution. DRIE etching results in vertical side walls, while wet etching follows the crystalline orientation of the silicon, which can result in sloped walls. In step 3.18d the micro channels are closed with another silicon wafer by bonding. The fusion bonding between two silicon wafers needs activated and very clean surfaces [63], and results in a strong bond up to the cohesive strength of the materials involved, step 3.18e. In step 3.18f the

thickness of the cover wafer has been reduced by mechanical grinding and CMP. Additionally an etching has been performed to open the inlet/outlet holes and to start the selective etching of the sensitive area. Step 3.18g shows the final product, the baseline cooling wafer, which has undergone another etching in the sensitive area and on top where the electronics will be sitting. All etching steps involve the repetition of steps 3.18a and 3.18b. In a last step, the wafer is diced to the desired shape.

(a) Photo-lithography mask

(b) Silicon wafer with resist mask

(c) Etching of Silicon wafer

(d) Closing of the channels with cover wafer by bonding

(e) Bonded cooling plate

(f) Etching to open connecting holes and grinding of cover wafer

(g) Selective etching in the sensitive area and to host the electronics

Figure 3.18: Simplified production process of a micro channel heat sink.

3.4 Micro Channel Testing

3.4.1 Thermal Mock-ups of the Sensor Assembly

The readout electronics (chip) and the pixel detector (sensor) were still under development during the development of the cooling system. Also the bump bonding process to combine 10 readout chips and the pixel sensor to a sensor assembly was under investigation. For the evaluation of the micro channel cooling plate and frame one needed to produce realistic dummy electronics. These mock-ups need to be as realistic as possible in dimensions and thermal behaviour and should deliver realistic temperature informations. The first mock-up was a Minco [10] flexible heater with roughly the dimensions of the ten readout chips, see figure 2.13. It was operated with a uniform power dissipation equal to the assumed average power dissipation of the chips. The temperature was measured with a thermal camera and Pt100 probes glued to the surface of the heater. As the chip design progressed, the choice of an EoC architecture made it clear that each chip would have two zones with very different heat flux densities. A more sophisticated dummy electronics design became necessary for a realistic mock-up with sufficient thermal information. Thermal mock-ups with progressively enhanced sophistication were designed by the CERN PH-ESE department [7] in collaboration with the UCL CP3 institute [4]. The kapton mock-up and the ceramic mock-up were produced by the PH-DT [6] Micro Pattern Technologies section. The silicon mock-up was produced in the EPFL CMi [1] in collaboration with CERN PH-DT [6].

The Kapton Mock-up

The kapton mock-up was the first attempt to create a thermal load on the cooling plate comparable to the chip configuration. Each chip has a zone with a high heat flux density with approximately $3.2\,\mathrm{W/cm^2}$, referred to as the digital zone, and a zone with low heat flux density with approximately $0.4\,\mathrm{W/cm^2}$, referred to as the analogue zone, see figure 3.10. As the ten chips are placed in two rows of 5 chips head to head, the digital heating zones are on the outside and analogue heating zones touch in the middle. So the kapton mock-up has 3 separate heating zones and 15 Pt100 temperature probes [84], 10 for the two

digital heating zones and 5 for the analogue heating zone. Figure 3.19 shows the top of the mock-up with the 15 temperature probes and their 4-wire connection on the left side. On the right side one can see the electric connection for the 3 heating zones.

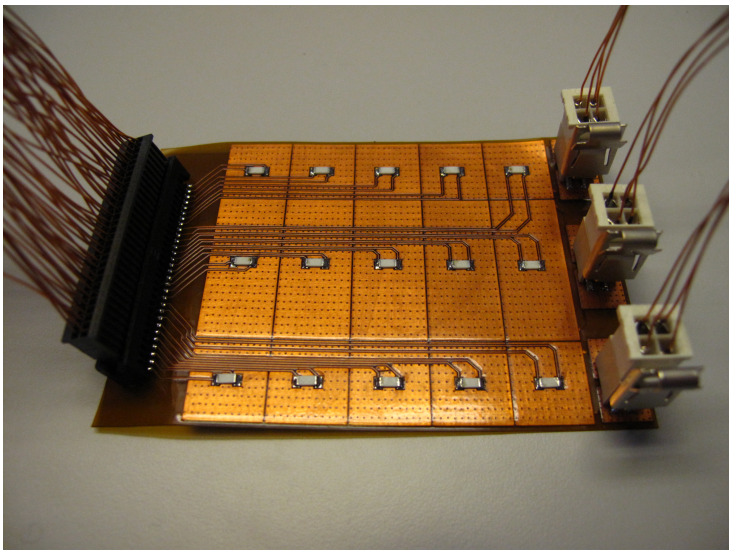


Figure 3.19: The kapton mock-up with 15 PT100 temperature probes and 3 heating zones.

Ceramic and Silicon Mock-ups

The ceramic and silicon mock-ups have the same layout concerning the distribution of heaters and temperature sensors. Also their geometric dimensions and their electrical layout are equal. The difference is the carrier material and the electrical resistances of the heaters. Both mock-ups have real dimensions concerning the thickness of the carrier material. The ceramic mock-up delivers very accurate results if mounted on the micro channel baseline cooling plate. The difference in thermal conductivity between the ceramic carrier and the silicon of the final sensor assembly can be neglected, due to the minimal thickness. The heat flow is almost exclusively perpendicular through the ceramic plates. Figure 3.20 shows a ceramic mock-up mounted on a micro channel baseline cooling plate. Each side, left and right, of the ceramic chip plate has 5 individ-

ual digital heaters and temperature probes. The 10 individual analogue heaters are under the ceramic sensor plate. Five temperature probes are mounted on the top centre.

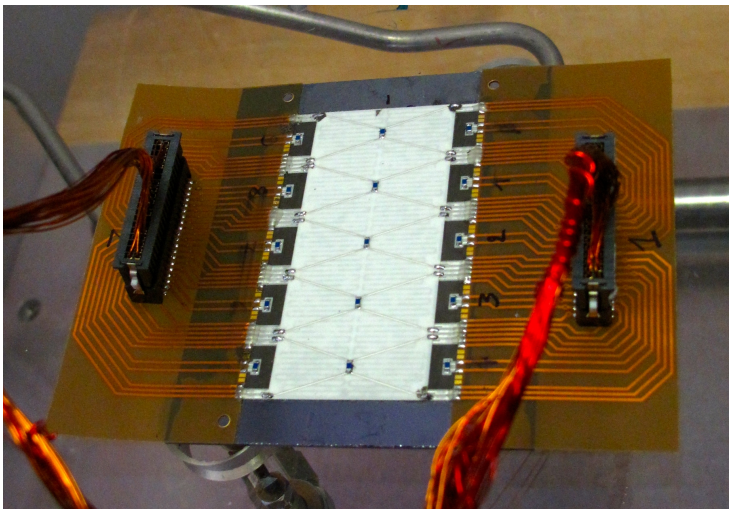


Figure 3.20: Ceramic mock-up glued on baseline mc cooling plate.

With the development of the micro channel cooling frame, the ceramic mock-up could not be used any more for testing; as the cooling frame concept relies on the capability of the carrier material to conduct the heat to the outside, where the frame touches the EoC region of the chip, the carrier material has to consist of the real material. The thermal conductivity of the ceramic material is approximately 55 W/mK at 0 °C, while the one of silicon is approximately 124 W/mK at 0 °C [57, 35]. Consequently the mock-up design was transferred to silicon as carrier material. Figure 3.21 shows a silicon chip plate with 20 individual heaters to simulate 10 readout chips (each one with two separate zone of power distribution) and a passive silicon sensor plate with electrical lines to connect 5 temperature probes on top.

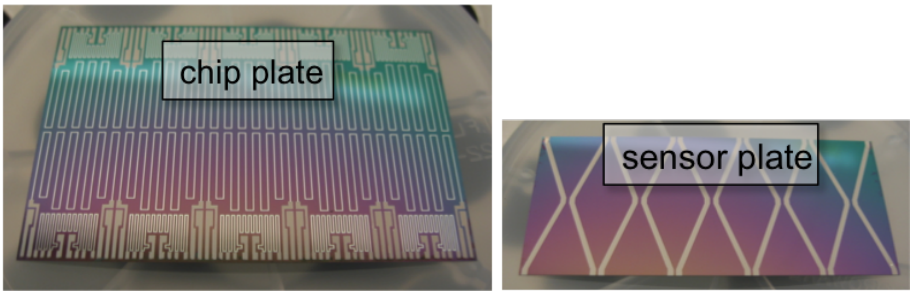


Figure 3.21: Silicon mock-up plates before glue assembly.

Figure 3.22 shows an assembled silicon mock-up, where chip plate and sensor plate glued together form the sensor assembly to simulate the chip-sensor bump-bond connection of the real detector. It has been equipped with 15 temperature probes, 10 in the 2 EoC regions and 5 on top of the sensor plate. Kapton extenders are soldered to the top and bottom. They connect the temperature sensors and the electric resistance heaters to the black 40 pin SAMTEC connectors vissible in the picture. The connectors can be soldered directly on top of the chip plate or they can be connected with small wires. Later on the micro channel cooling plate together with the thermal mock-up will be installed into a test PCB, see Figure 3.23, where the electrical connection can also be done with wire bonding [64].

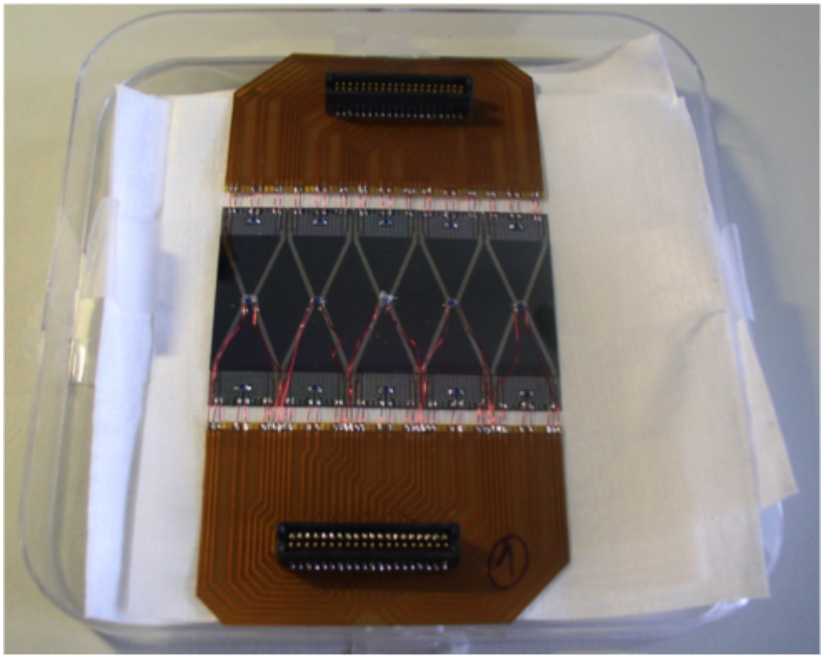


Figure 3.22: Silicon mock-up assembled and equipped with temperature sensors.

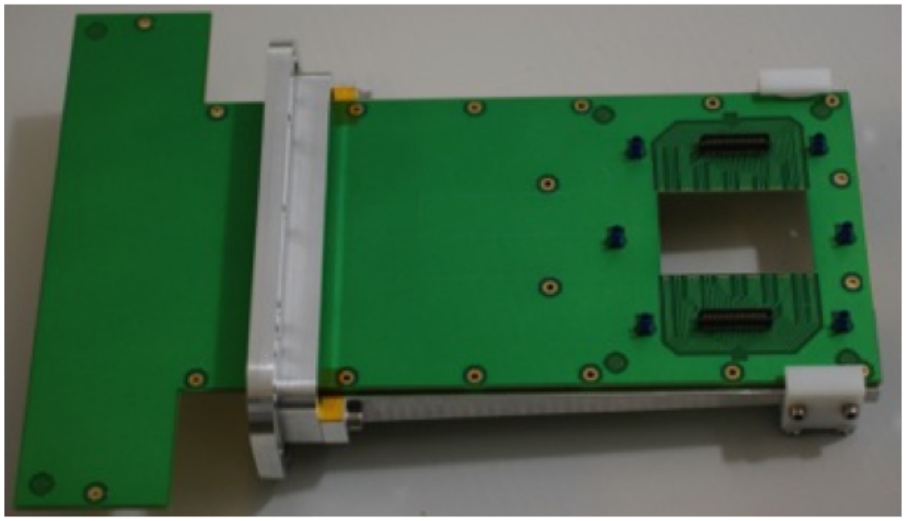


Figure 3.23: PCB for micro channel cooling and assembly tests.

To further approach to the reality of the detector, the silicon mock-up has to be produced with 10 separate chips, see figure 3.24. They can be produced by dicing a silicon chip plate, figure 3.21. For the thermal testing of the baseline micro channel cooling plate or the alternative micro channel cooling frame at their design condition single mock-up chips are in principle not necessary. The transversal heat flux inside the silicon is minimal compared to the heat flux through the silicon. However, this better allows for testing in realistic off-design conditions, like loss of one or more chips in the detector. For integration tests on the other hand single silicon mock-ups can become necessary in any case.

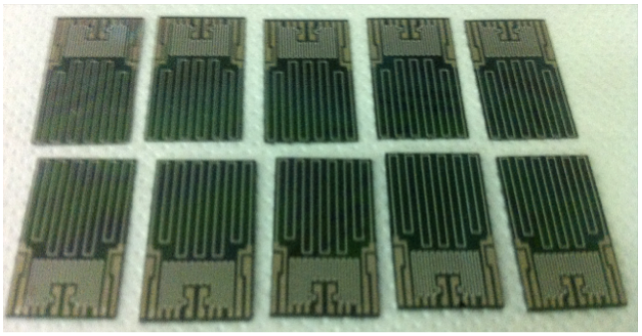


Figure 3.24: Silicon mock-up assembled and equipped with temperature sensors.

The temperature measurement in all mock-ups used PTS SMD Flat Chip resistive temperature probes from Vishay, class F0.3 [84]. The probes are based on the Pt100 principle and have an error of $\pm 0.3\,\mathrm{K}$ at $0\,^{\circ}\mathrm{C}$. Between the SAMTEC [11] connector and the readout cards of the National Instruments [8] chassis, the connection is realized in the 4-wire method, see 3.4.2. Between the SAMTEC connector and the Pt100 probe the connection is done in 2-wire method. The reason is the complex design of the mock-up. There was not enough space to realize a 4-wire connection up to the temperature probe. The additional resistance from the electric lines between the SAMTEC connector and the Pt100 probe is subtracted from the temperature values during the analysis of the data. The results presented in Chapter 4 are all based on measurements with the silicon mock-up.

3.4.2 Test Stand

The micro channels test stand is composed of the actual test section, the test rack, the cooling plant and the data acquisition. The hydraulic piping scheme and the wiring scheme of the electronic mock-ups can be seen in Appendix A.

Test Section - Vacuum Vessel

The test section is a vacuum vessel, shown in 3.25. The vessel design is based on a similar PH-DT design and the design has been adapted by the UCL CP3 design office. It was then produced in the UCL workshop before shipping. The vessel was then equipped and commissioned at CERN by PH-DT and UCL CP3. The micro channel object to be tested is placed on a holder (transparent plexiglas) and is then connected to the hydraulic C_6F_{14} circuit. On the left side one can see the fixed lid of the vessel. It contains the hydraulic and electric feedthroughs. The right part of the vessel can slide for opening and closing. On the right side of the vessel one can see the installations to generate a vacuum. It includes valves to separate the vessel, a vacuum probe and tubing to connect to a turbo molecular pump. On the top of the vessel is a sight glass for visual inspection of the test object under vacuum.

Figure 3.26 shows the outside of the vessel under closed conditions. Visible on the left are the two Swagelok pressure probes on inlet and outlet [72]. The inlet pressure probe has a range from 0 bar to 25 bar and the outlet pressure probe has a range from -1 bar to 25 bar. Both pressure probes have an accuracy of $\pm 0.5\%$. One can also observe a bypass to cool down the pipes more quickly at initialization.

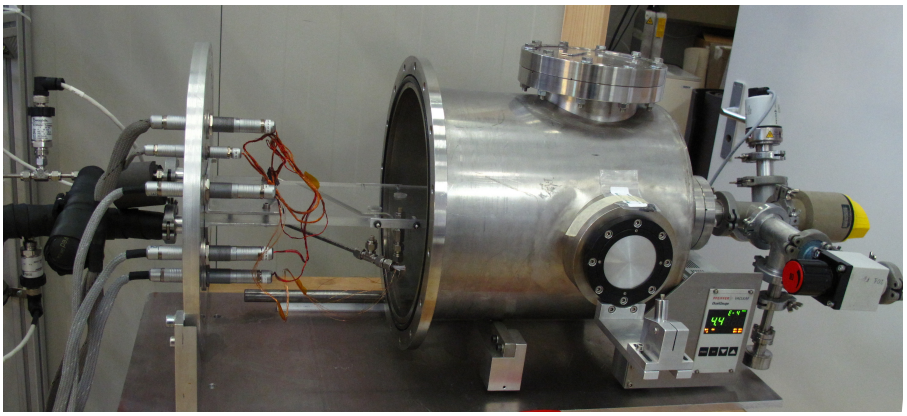


Figure 3.25: The vacuum vessel fully equipped before closing.

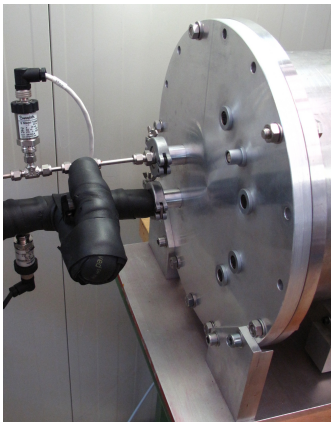


Figure 3.26: The lid of the vacuum vessel.

Test Stand Rack and Cooling Plant

The design of the test stand rack for micro channel experiments is shown in figure 3.27. It was build by PH-DT gas systems team. On top of the rack is the National Instruments (NI) [8] chassis of the DAQ system. Temperature probes, pressure probes and reading of the heating power are connected via cables to the cards inside the chassis. The National Instruments chassis is then connected via a USB cable to a desktop computer for data reading.

Below stands the Krohne Optimass 3000 flow meter [49]. It measures the flow rate between 0.5 and 36 g/s with an accuracy of $\pm 0.1\%$. In front of the flow meter is a panel that allows the 20 individual heaters of the thermal mock-up to be switched on and off individually. Below the mass flow meter is another panel that contains two metering valves and two analogue pressure probes. The two metering valves control the flow to the test section and through a bypass. There is an electric switch box located underneath. A booster pump is installed on the bottom of the rack. This gear pump raises the pressure of the incoming C_6F_{14} flow from the 4 bar delivered by the C_6F_{14} cooling plant up to 12 bar with the fluid at room temperature. Furthermore the test rack contains piping, ball valves, safety valves, pressure and temperature probes to control the flow.

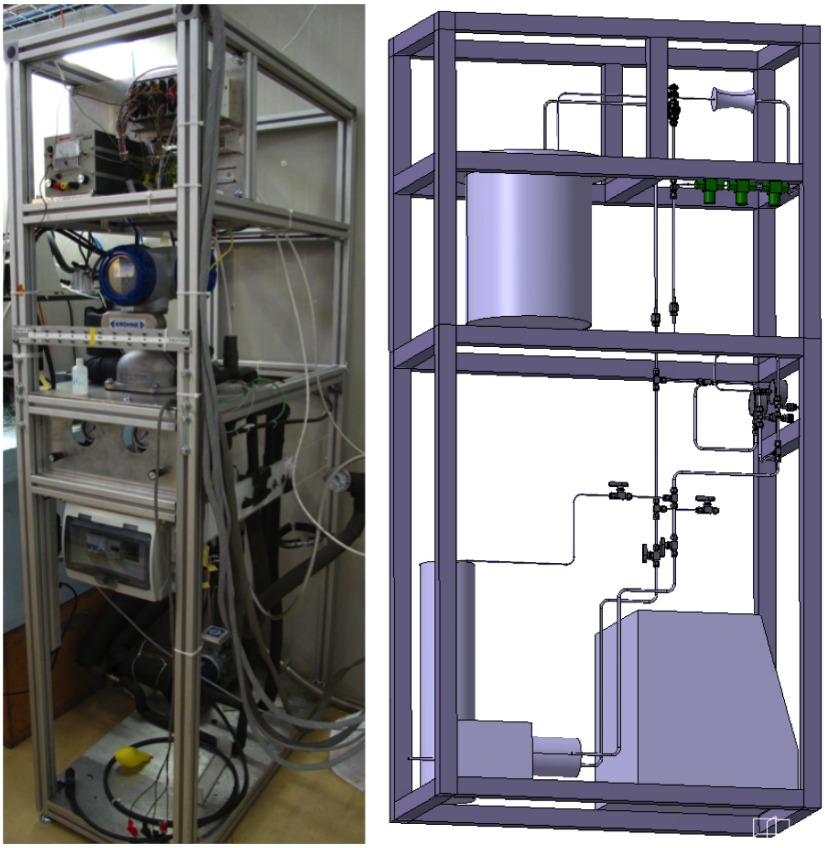


Figure 3.27: Micro channel cooling test rack in the lab and as 3D model

The C_6F_{14} cooling plant is shown in figure 3.28. It had been recuperated from the CMS pixel test facility. It was used to cool parts of CMS pixel detector during the test and commissioning phase. For the cooling of the GTK detector it is far too powerful. As a consequence, it has been equipped with an internal bypass and a additional heat load. The heat load is necessary to guarantee a stable long run of the cooling plant. Without the heat load, the refrigeration unit switches on and off, which can overstress the compressor valves.

Figure 3.28: CMS pixel test cooling plant.

Data Acquisition

The data acquisition (DAQ) is realized with a National Instruments chassis [8]. It is connected via USB to a computer running the NI-software LabView. The rack contains 8 slots for readout cards. 4 RTD (Resistance Temperature Device) cards read the Pt100 temperature probes. Per card 4 Pt100 temperature probes can be read. One multipurpose card reads 2 Pt1000 sensors at inlet and outlet. The temperature sensors are connected in 4-wire mode from the NI cards up to the heater connections, including the vacuum feedthroughs. One card processes signals in the $4 - 20\,\mathrm{mA}$ range. The mass flow meter, the 2 pressure sensors and the 2 power supplies deliver their data in this range. Figure 3.29 shows the graphical user interface of the LabView program. All data are monitored during the tests and saved in a text file with a sample rate of $1/\mathrm{s}$. These files are then used to extract the individual data points. One data point is defined as

the average data over 2 minutes, which means 120 single data points. In these 2 minutes all relevant parameters are kept constant. The resulting data points are then used to perform the analysis and extract the thermal and hydraulic behaviour.

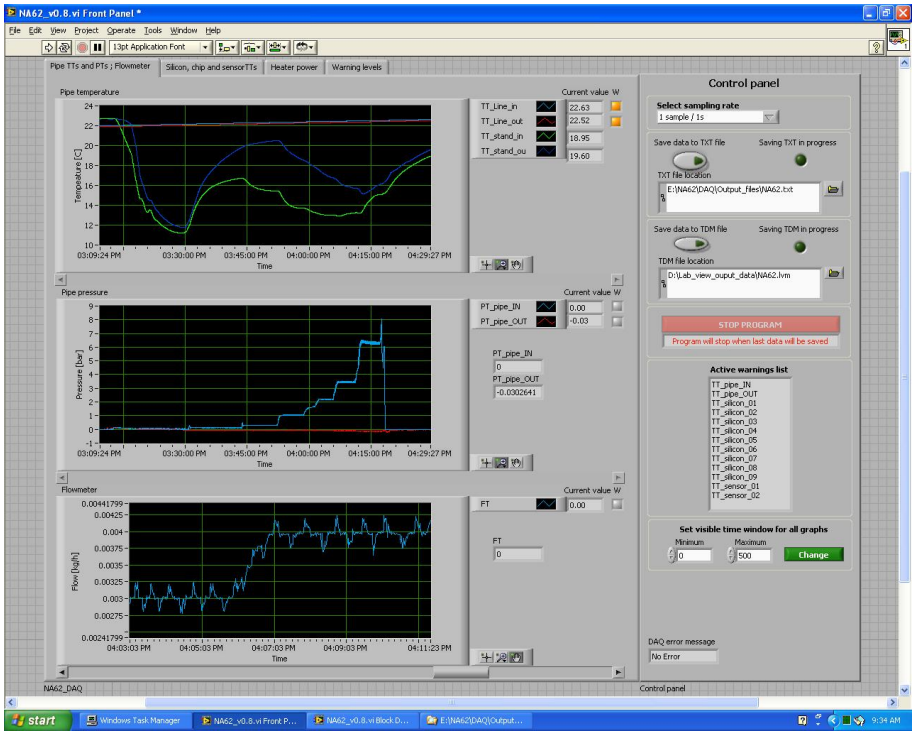


Figure 3.29: DAQ: LabView graphical user interface

4 Results of Baseline Cooling Plate and Alternative Cooling Frame

This chapter will present the thermal and hydraulic results of the baseline cooling plate and the alternative cooling frame. The results have been obtained in tests, which have been carried out in the test stand, described in 3.4. Figure 4.1 shows the simulated power output of the TDCpix in 2013. In this chapter, the heat loads for the silicon mock-ups, referred to as nominal and maximum, are based on this estimation.

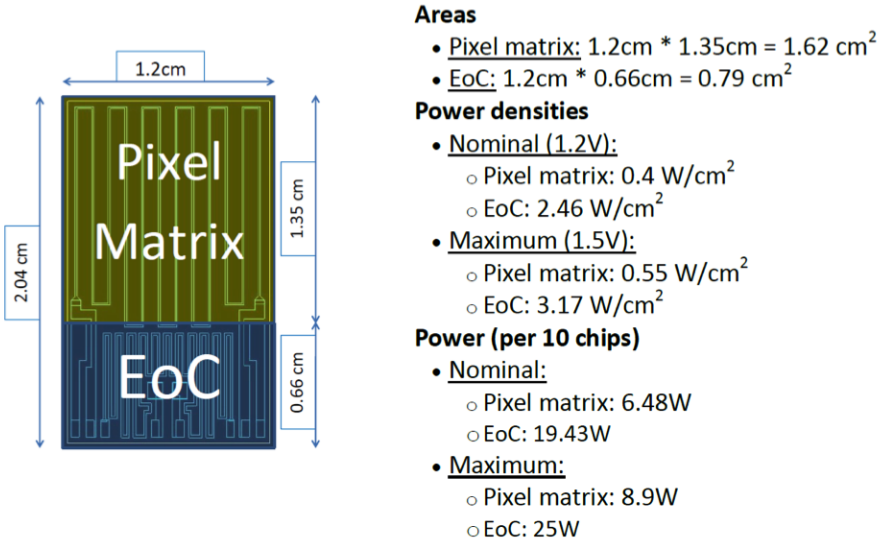


Figure 4.1: Simulated thermal power output of the TDCpix in 2013 and electrical power input into the mock-up electronics.

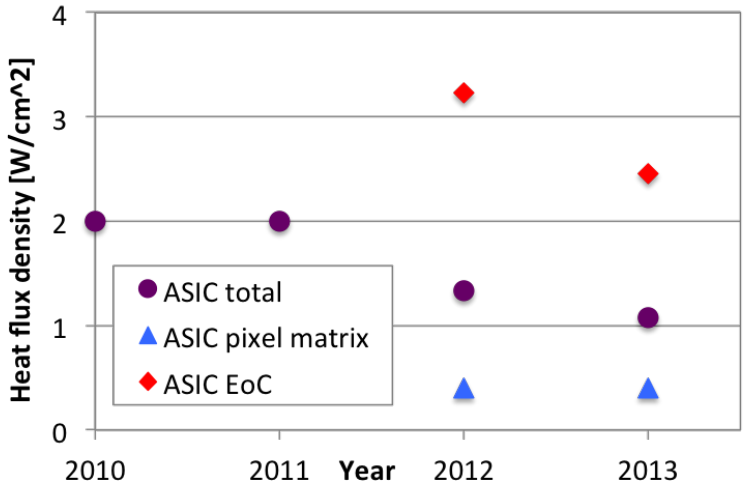


Figure 4.2: Predicted or simulated heat flux density of the TDCpix for nominal power settings over the time of the project.

The graph of figure 4.2 shows the predicted or simulated nominal heat flux densities of the readout chip, which was under development. By the end of 2011 the EoC design was chosen for the TDCpix readout chip, see 3.2. Although the total heat flux density went down, the EoC region shows a significantly higher heat flux density. This higher heat flux density leads to a higher temperature difference between micro channel heat sink and electronics, which can result in higher thermal stress or deformation. Therefore it is important to look at this region in the micro channel design and testing phase.

Figure 4.3 explains how the 20 single heaters on the mock-ups represent the geometric arrangement of the 10 TDCpix chips that will be bump bonded under the pixel sensor. The upper row of 5 chips can be mirrored at the lower end of the pixel matrix to get the lower row of 5 chips. In this way one receives 2 EoC regions on top and bottom and one combined pixel matrix region in between. The 3 regions feature a constant heat flux density within.

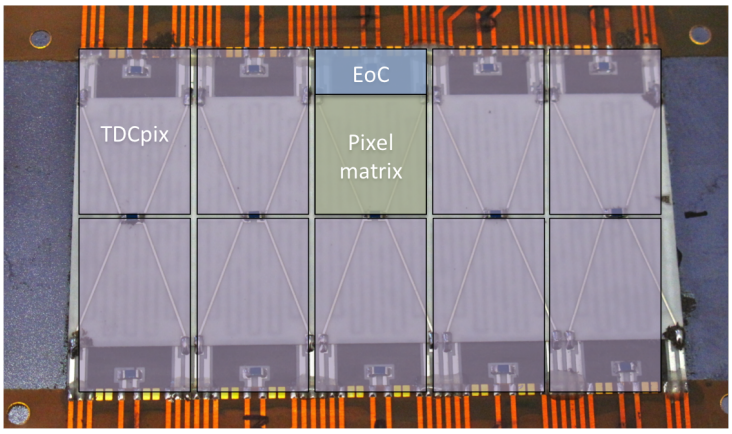


Figure 4.3: Mock-up electronics: configuration of the 10 TDCpix compared to the heaters on the mock-ups.

4.1 Baseline Cooling Plate

4.1.1 Hydraulic Behaviour

The baseline cooling plate, shown in figures 3.7 and 3.8, has an almost equal flow distribution over the channels and a low pressure drop. An equal flow distribution guarantees a uniform temperature distribution over the cooling plate. Figure 4.4 shows qualitatively the mass flow distribution over the channel area. It shows the result of a simulation for 300 channels with a cross section of 100 µm by 100 µm . Therefore the absolute numbers of the mass flow per channel are not representative for the baseline design, where the channels have a cross section of 200 µm by 70 µm . Nevertheless, the mass flow distribution over the channel area is comparable to the one in the baseline design.

Clearly visible are the 2 independent channel areas due to the double inlet/outlet design. The difference in mass flow over all channels is around 20%, with a maximum of approximately 0.029 g/s and a minimum of approximately 0.024 g/s for the configuration simulated. The difference in mass flow can be explained with the flow conditions, especially in the inlet manifold. Here the flow enters with a high velocity and high pressure. The flow is turbulent when it enters the manifold and produces a high pressure drop. This means that

the total pressure inside the inlet manifold decreases significantly along the flow direction. As a result the mass flow through each channel drops in the direction of the flow through the manifold, since the available pressure drop to drive the flow through each channel decreases. A larger manifold would reduce this effect, but due to constraints in material budget, mechanical stability and connector size, one can not design the manifolds larger. Depending on the manifold and channel design, the total channel cross section (all channels) is between 10 and 15 times larger than the manifold cross section. This shows the dilemma of the integration of the manifolds in the micro channel heat sink. Ideally the manifold cross section should be greater than or equal to the total channel cross section [85, 79].

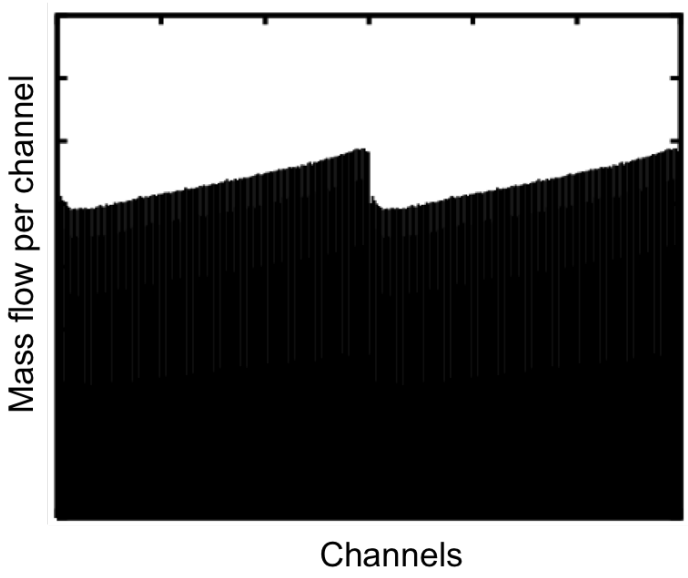


Figure 4.4: Qualitative mass flow distribution over the channel area [32].

Figure 4.5 shows the measured pressure drop of the baseline cooling plate over the mass flow. For the corrected value the additional pressure drop of the tubing between the 2 pressure probes is subtracted. The additional pressure drop, of the tubing only, at different mass flows and temperatures, had been measured during the calibration of the test stand. From these values an empirical equation was derived that calculates the pressure drop originated by the tubing

at the measured data point. The error bars show the accuracy of the mass flow meter and the pressure probes magnified with the factor 10.

A pressure drop of approximately 8 bar, for the maximum mass flow approximately 10 g/s, is no problem for the cooling plate. The highest pressure occurs only in the 2 inlet manifolds. Since the manifold region is not affected by the selective thinning in the center of the baseline design, the silicon is thicker and stronger to withstand the pressure. In the thinned area, the geometrical dimensions are small enough to reduce the stress on the silicon.

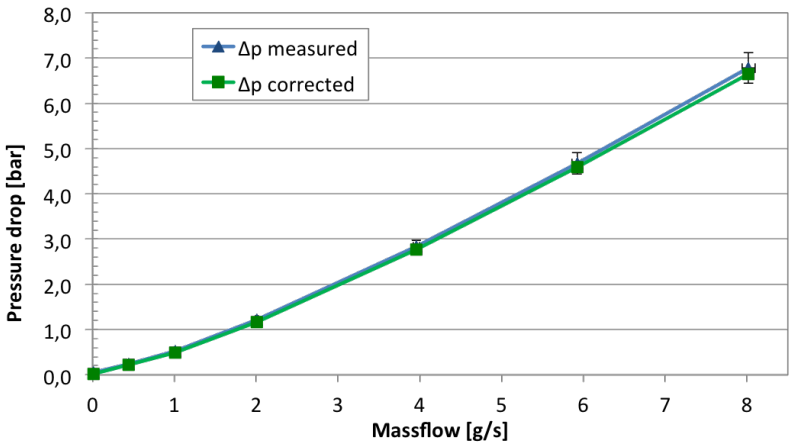


Figure 4.5: Measured and corrected pressure drop of the baseline cooling plate at -20 °C set point temperature of the cooling plant.The error bars on the measured values are magnified 10 times to make them visible.

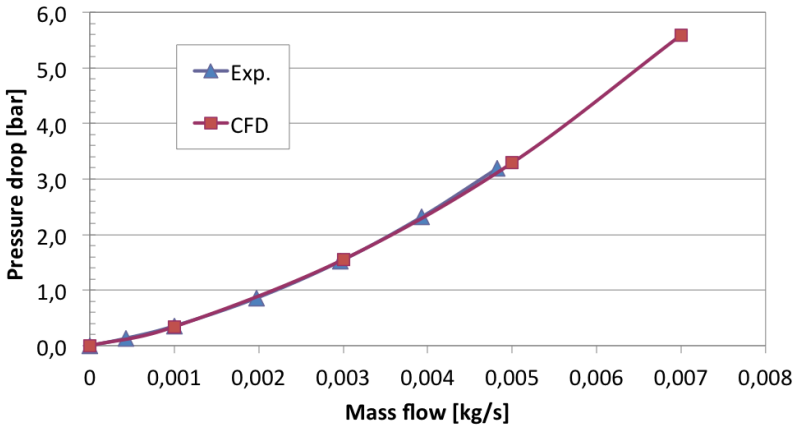


Figure 4.6: Measured and simulated pressure drop of the baseline cooling plate at 15 °C inlet temperature.

Figure 4.6 shows the excellent pressure drop prediction of CFD simulations. The experimental data were taken at 15 °C inlet temperature in ambient atmosphere. In the simulations, the temperature of the coolant was fixed to 15 °C.

4.1.2 Thermal Behavior

The cooling of the GTK subdetector needs to keep the temperature at the silicon pixel sensor in a range of ±3 °C and below 5 °C , although a lower temperature is preferred. The thermal results presented in the following graphs have been measured with a constant C_6F_{14} mass flow of approximately 7.6 g/s. The inlet temperature to the test section was kept constant at -21.3 °C. Figure 4.7 illustrates geometric distribution of the temperature probes on top of the silicon mock-up. The top picture shows 3 different heating zones with different power densities, namely an upper digital zone, an analogue zone and a lower digital heating zone. In the lower picture the numbering of the temperature probes and the inlet/outlet configuration is given. It is a counterflow configuration. Other configurations are possible, but were not tested with this prototype. Figure 4.8 shows a numbering scheme used when temperature results of each zone are combined in one graph.

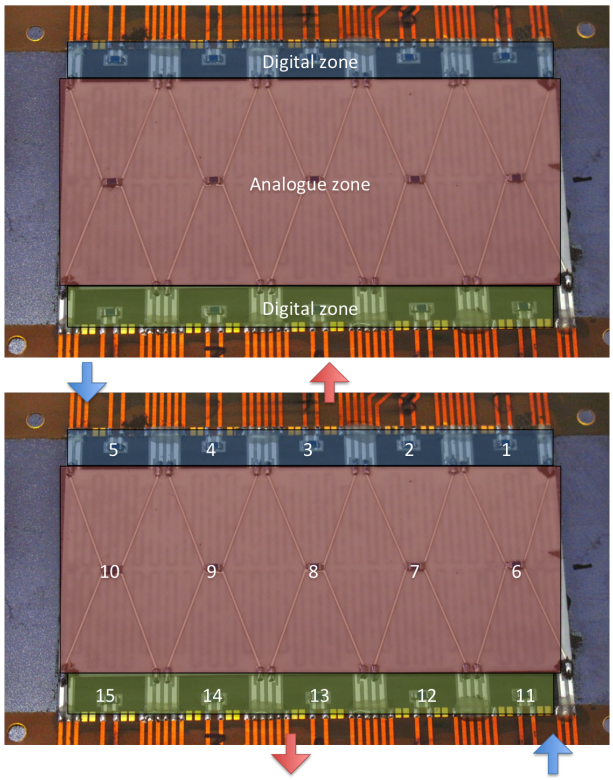


Figure 4.7: Silicon mock-up: zones and numbering of temperature probes and inlet (blue arrow) and outlet (red arrow) configuration.

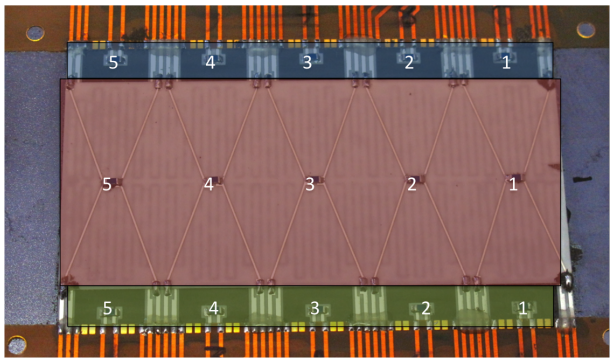


Figure 4.8: Silicon mock-up: alternative numbering of temperature probes, if results from the 2 digital zones and the analogue zone are combined in one graph.

The legend in figure 4.10 contains the color coding of the power settings and is also valid in figures 4.9 and 4.11. The power settings do not correspond to the thermal power output presented in figure 4.1 since they are based on an earlier simulation of the TDCpix. The power settings used in these test cover the settings assumed in figure 4.1 and represent the possible range of power output.

The graphs in figures 4.9, 4.10 and 4.11 show that for all power settings, the pixel sensor temperature can be kept at below -13 °C and in a range of ±1 °C. This corresponds very well with demands in temperature stability for the GTK subdetector. The temperature variation along the sensor surface is caused by the counterflow configuration. A parallel flow configuration will minimize the temperature variations along the sensor surface and a long the digital zones. The digital zones show a larger temperature variation. The limit of the temperature range of ±3 °C is kept in most power settings. The highest temperature difference along the digital zones is 7 °C. A parallel configuration would lead to a cold digital zone, a medium analog zone and a warmer digital zone. The extreme power of 40 W in the digital zone could cause a problematic thermal expansion with high stress or breaking. A test with a parallel flow configuration with this cooling device and heater was not possible.

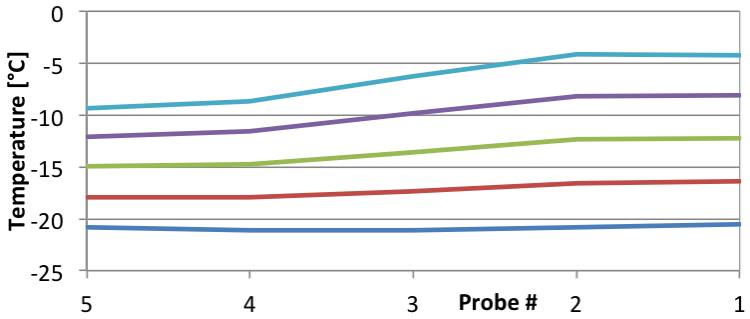


Figure 4.9: Temperatures of the upper digital part for different power settings. (see figure 4.10 for the legend)

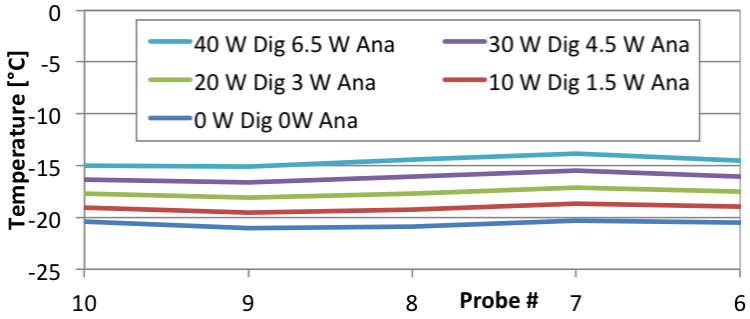


Figure 4.10: Temperatures of the analogue part for different power settings.

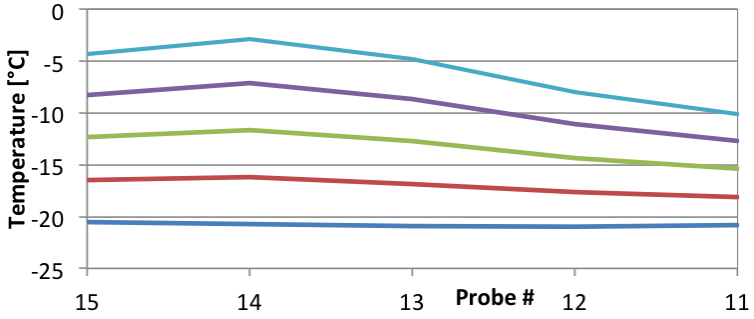


Figure 4.11: Temperatures of the lower digital part for different power settings. (see figure 4.10 for the legend)

To give an idea of the temperature distribution in case of the nominal power setting, see figure 4.1, one can combine the results of the green lines for the digital zones and the results of the light blue line for the analogue zone. This means that the two digital zones produce 20 W and the analogue zone 6.5 W heating power. The result is shown in figure 4.12. The color coding and the numbering corresponds to the ones in figure 4.8. In reality the temperature variation in the analogue zone will be smaller, like the one of the green line in figure 4.10. The numbering of the temperature probes is correct for the upper digital zone. For the other 2 zones the probe numbering corresponds to the numbering in figure 4.8.

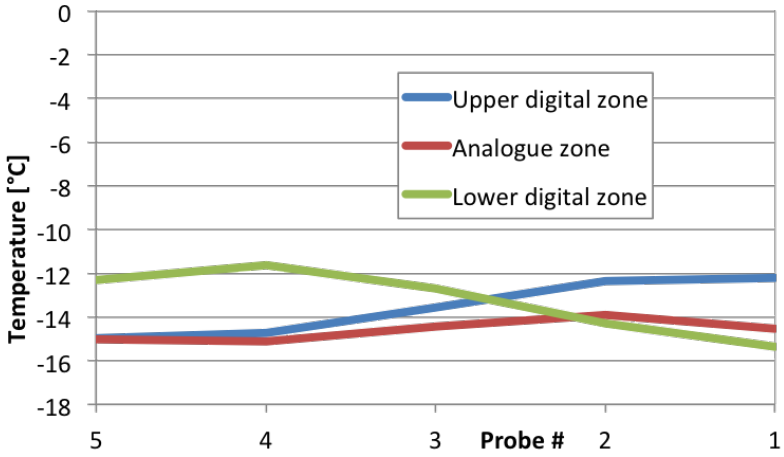


Figure 4.12: Temperatures of silicon mock-up with combined nominal power settings.

A parallel flow configuration will reduce temperature variation and consequently the thermal stress in the cooling plate and the sensor assembly. Other prototypes could prove the concept, but the thermal results were incomplete due to the failure of several single heaters on the silicon mock-ups. The thermal pictures presented in section 4.3 manifest that a parallel flow configuration reduces the temperature variations.

4.2 Alternative Cooling Frame

4.2.1 Hydraulic Behavior

In the case of the micro channel cooling frame the pressure drop of the fluid is less critical. Since the material under the EoC region of the TDCpix can be much thicker, also the channels can be deeper. This leads to the lower pressure drop of the cooling fluid at the nominal mass flow. As a reminder, figure 4.13 shows the geometry of the frame and its position under the EoC region. The channels are 100 µm wide and 300 µm deep, with 25 µm wall thickness between channels.

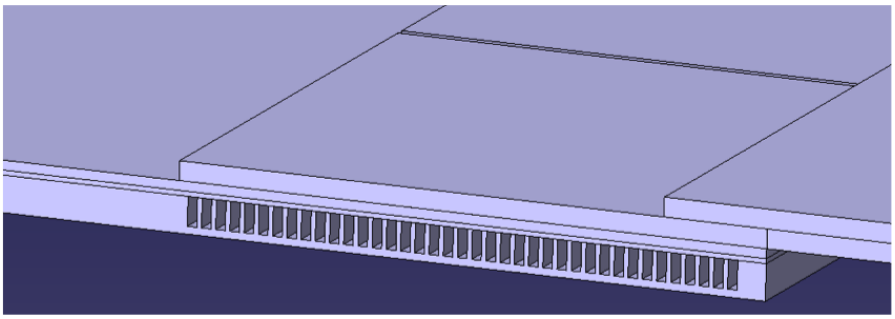


Figure 4.13: 3d Catia model of the cooling frame, the readout chips and the pixel sensor, cut in the center.

The pressure drop of the cooling frame, where the liquid runs under the two EoC regions, is shown in figure 4.14. For the corrected pressure drop value the additional pressure drop of the tubing between the 2 pressure probes is subtracted, see 3.1. The error bars show the accuracy of the mass flow meter and the pressure probes magnified with the factor 10.

The pressure drop of approximately 3.5 bar at 10 g/s mass flow is in no way critical for the mechanical stability of the cooling frame. In case of the frame, it is more important to have a large inner surface of the micro channels to enhance the heat transfer between silicon and C_6F_{14}.

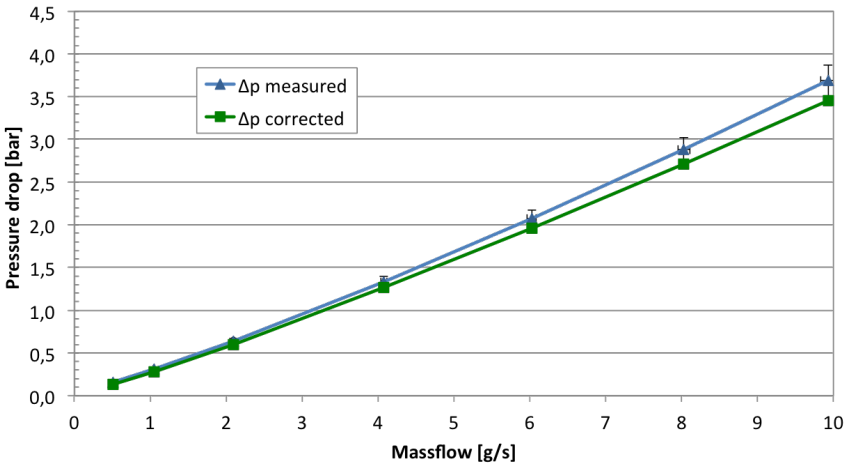


Figure 4.14: Measured pressure drop of the alternative cooling frame at -20 °C fluid inlet temperature. The error bars on the measured values are magnified 10 times to make them visible.

4.2.2 Thermal Behaviour

Thermal behaviour of the frame is significantly different than the one of the baseline. While the baseline cooling plate keeps the pixel sensor at a stable and low temperature, the cooling frame only cools the EoC region of the TDCpix and relies for the cooling of the pixel matrix and the pixel sensor on the thermal conduction inside the pixel matrix to the Eoc region. Therefore it is necessary to limit the chip thinning to a thickness of 200 µm instead of 100 µm for the baseline cooling plate. This doubles the cross section used for thermal conduction. All thermal results for the frame have been acquired with mock-up electronics in which the chip plate, see figure 3.21, has a thickness of 200 µm .

The numbering of the temperature probes for the following results follows the scheme in figure 4.15. The blue arrows mark the inlet position and the red arrows the outlet position. The flow configuration is parallel. The 2 orange boxes at the positions of temperature probe 4 and 15, mark 2 heaters in the digital zones that did not work during the tests. Due to a problem during the microfabrication of the silicon mock-ups a lithography mask with an imperfection was used. This lead to a batch of silicon mock-ups with a systematic

failure of these 2 single heaters. However, the silicon mock-ups where used anyway to quickly prove the concept of the cooling frame.

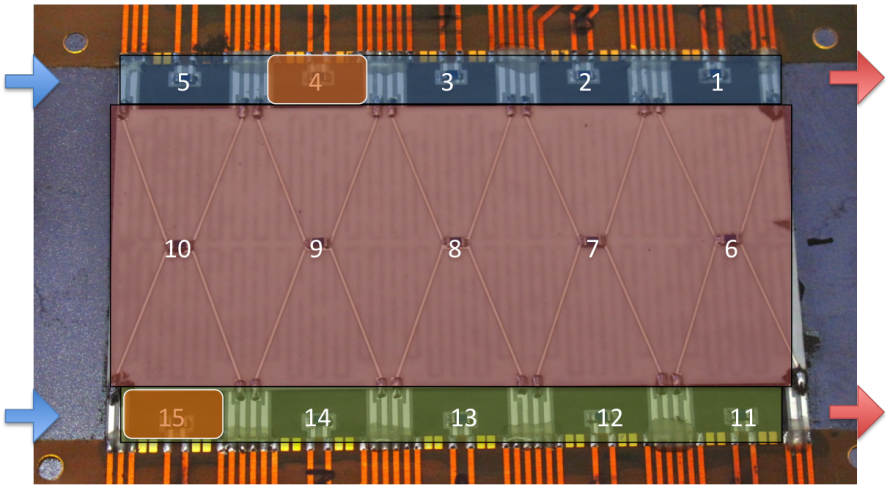


Figure 4.15: Silicon mock-up: numbering of temperature probes, flow direction and inlet/outlet (blue/red arrows) configuration and marking of 2 broken heaters in the digital zones.

The legend in figure 4.16 contains the color coding of the power settings and is also valid in figures 4.17 and 4.18.The power settings do not correspond to the thermal power output presented in figure 4.1, since they are based on an earlier simulation of the TDCpix and are adapted to the failure of the 2 single heaters in the 2 digital zones.

The following results of the thermal behaviour where measured with a mass flow of 10 g/s and an inlet temperature of -21 °C. The graphs in the figures 4.16, 4.17 and 4.18 show that for all power settings, the pixel sensor temperature can be kept at below 5 °C and in a range of ±3 °C. The temperature rise is caused by the parallel flow configuration from left to right. The digital zones are less sensitive in terms of temperature, to power changes since they are cooled in direct contact.

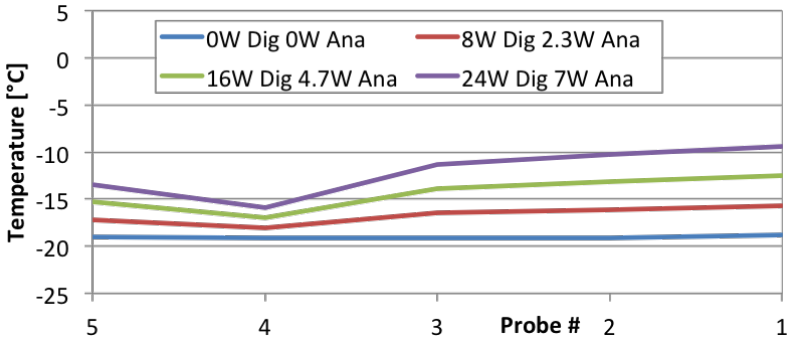


Figure 4.16: Temperatures of the upper digital part for different power settings.

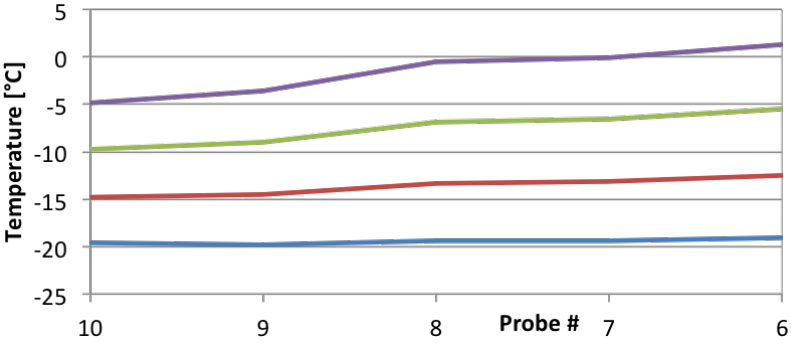


Figure 4.17: Temperatures of the analogue part for different power settings. (see figure 4.16 for the legend)

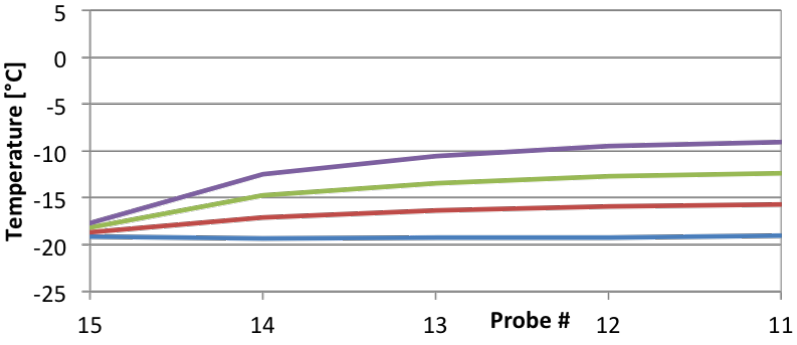


Figure 4.18: Temperatures of the lower digital part for different power settings. (see figure 4.16 for the legend)

The violet lines of the graphs in the figures 4.16, 4.17 and 4.18 represent results that are closest to the nominal power setting in figure 4.1. Here the two digital zones produce 24 W and the analogue zone 7 W heating power, which is a slightly higher heat production than predicted for the nominal power setting. The 3 resulting curves are shown in figure 4.19. The color coding corresponds to the 3 zones in figure 4.7. The numbering of the temperature probes corresponds to the numbering in figure 4.8. It is clearly visible that with a quasi nominal power setting the analogue zone is warmer than the digital zones. To reach the desired operation temperature for the pixel sensor, one has to adjust the inlet temperature of the coolant to circa -25 °C. The use of a counter flow configuration will further reduce the temperature variation in the analogue zone, see figure 4.21.

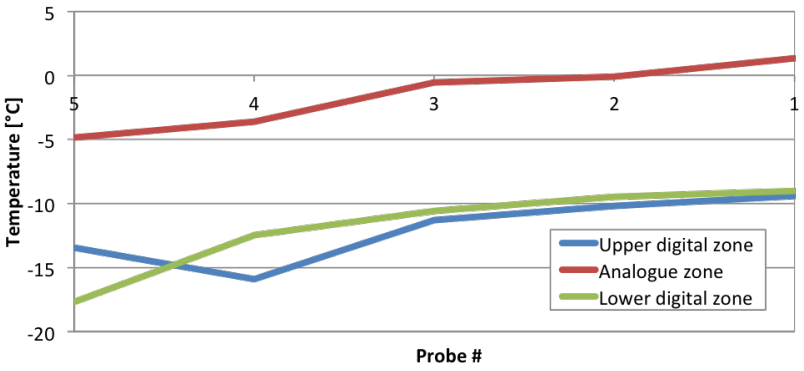


Figure 4.19: Temperatures of silicon mock-up with quasi nominal power settings.

The 2 curves of the digital zones are obviously disturbed by the 2 broken heaters. They should be rising straight and very close to each other. By replacing the value of temperature probe 15 (broken heater) with the value of temperature probe 5 (working heater) one can approximate the temperature behaviour of one fully working digital zone. The temperature behaviour of the analogue zone simply follows the inlet temperature. These 2 effects are visible in figure 4.20.

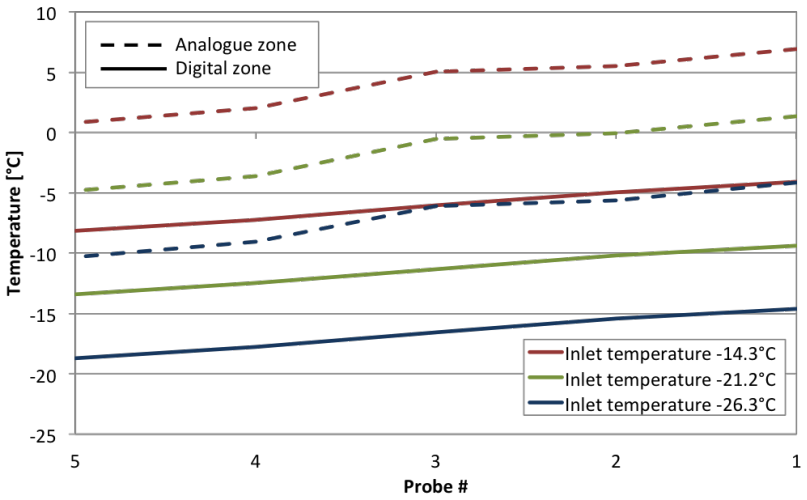


Figure 4.20: Measured temperature of the analogue zone and approximated temperature of on digital zone with quasi nominal power settings at different inlet temperatures.

The parallel flow configuration, presented so far, causes a rise of the analogue temperature in flow direction. A counter flow configuration can prevent that. The temperature of the pixel sensor would become more constant. A visual comparison of the 2 flow configurations can exemplify this best. Figure 4.21 compares the thermal image of a parallel flow with that of a counter flow. The thermal images were taken in ambient conditions at around 24 °C and with the same power settings. They overlay a picture of a mc cooling frame. The blue arrows mark the inlets and the red arrows the outlets. They also show the flow direction. The blue lines in the middle of the thermal images mark the geometric position at which the temperatures were read. These are plotted in the graphs underneath. The inlet temperature was kept at 15 °C in both cases to avoid condensation. The 2 heaters in the digital zones, marked in figure 4.15, do not work here either.

The conclusion from the thermal images and the graphs is that a counter flow configuration keeps the temperature variation in the analogue zone smaller than the parallel flow configuration. It is visible, even though the 2 digital heaters do not work. This means the counter flow configuration keeps the pixel sensor thermally more stable.

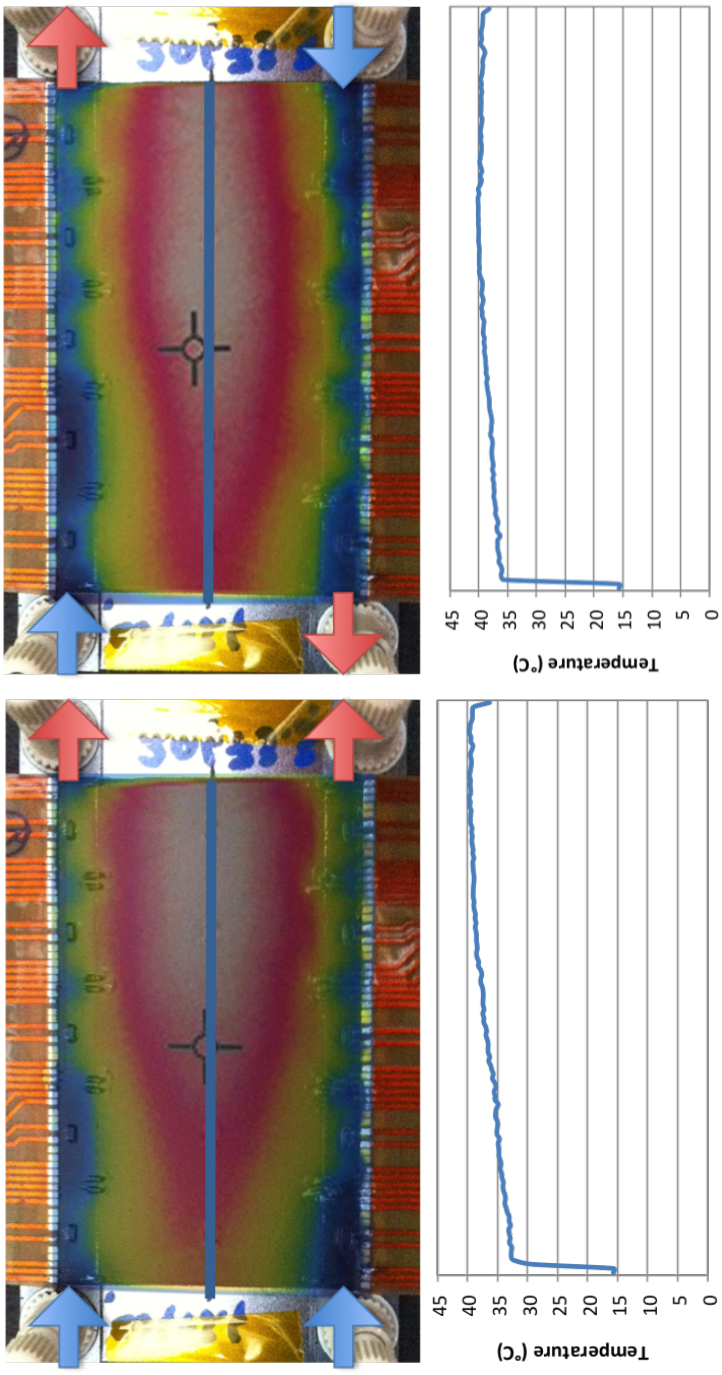


Figure 4.21: Comparison of parallel and counter flow configuration. The thermal images overlay pictures of the same cooling frame. Thermal images were taken in ambient condition. Power settings are the same in both cases.

4.3 Comparison of Cooling Plate and Cooling Frame

Thermal imaging is used for a visual comparison between the two heat sink concepts. The thermal images show the thermal behaviour of the silicon mock-up, cooled by the baseline cooling plate or the alternative cooling frame. The shiny surface of the silicon mock-ups does inhibit the correct temperature reading with a thermal camera. Instead the thermal camera reads the temperature of objects that reflect on the surface. Therefore it is necessary to paint the surface of the silicon mock-up. Matt black acrylic paint was sprayed on the surface. Figure 4.22 shows a baseline cooling plate and an alternative cooling frame with black painted mock-ups glued on top. In the picture of the frame, there are 3 heaters marked with orange boxes. These did not work during the tests. Two heaters in the analogue zone and one in the lower digital zone had an electrical problem.

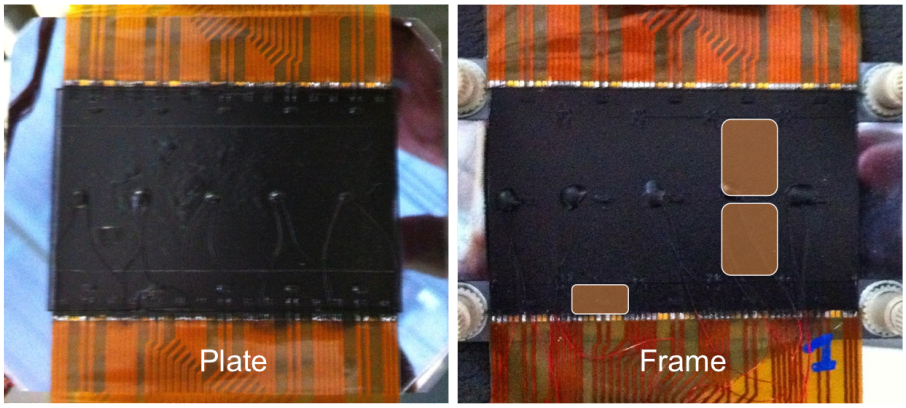


Figure 4.22: Baseline cooling plate and alternative cooling frame with black painted silicon mock-ups.

Figure 4.23 is the legend that belongs to the temperature range used in the thermal images underneath. The temperatures in the images should be seen as temperature differences to the inlet temperature T_{in} of 15 °C. The absolute temperature of the mock-up and with it the temperature of the sensor assembly can be regulated with the inlet temperature.

Figure 4.23: Legend for the temperature range in the thermal images.

Figure 4.24 shows the thermal image, when the cooling is running and the mock-up is not powered on. The blue arrows indicate the flow direction. The cooling plate is supplied in a parallel flow regime, while the cooling frame is supplied in a counter flow regime, which are the optimal flow regimes for the 2 heat sinks, respectively. The mass flow through the baseline cooling plate was 8 g/s and through the alternative cooling frame was 10 g/s. The images show that in both cases the temperature of the silicon mock-ups is kept at T_{in}. The thermal images were taken in an ambient environment at approximately 24 °C. These thermal images could not be taken inside the vacuum chamber.

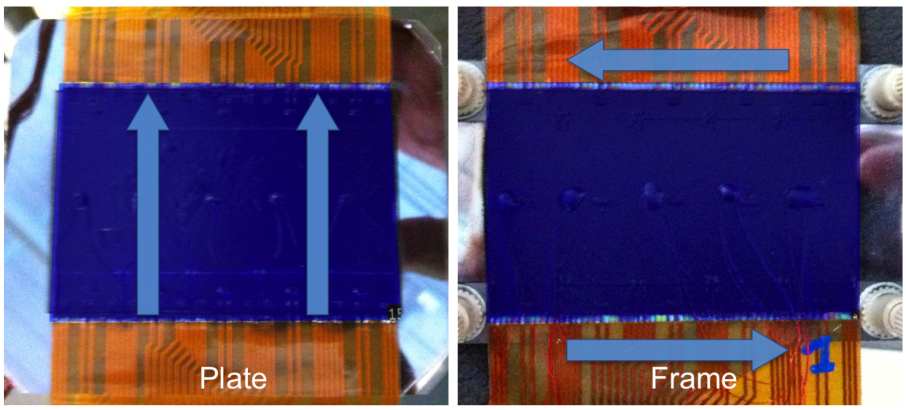


Figure 4.24: Cooling plate and cooling frame without power on silicon mock-ups. Coolant runs with 15 °C inlet temperature.

The power settings in figure 4.25 are as close as possible to the nominal power settings, and factor in the 3 broken heaters. The digital zones dissipate 18 W and the analogue zone dissipates 4.5 W. The cooling plate keeps the analogue zone at an equal temperature of approximately 5 °C above T_{in} and the digital zones at approximately 12 °C above T_{in}. The cooling frame in the contrary keeps the analogue zone at approximately 15 °C above T_{in} and the digital zones slightly colder around 10 °C above T_{in}. The temperature distribution of the

analogue zone would be more equal if all heaters would work.

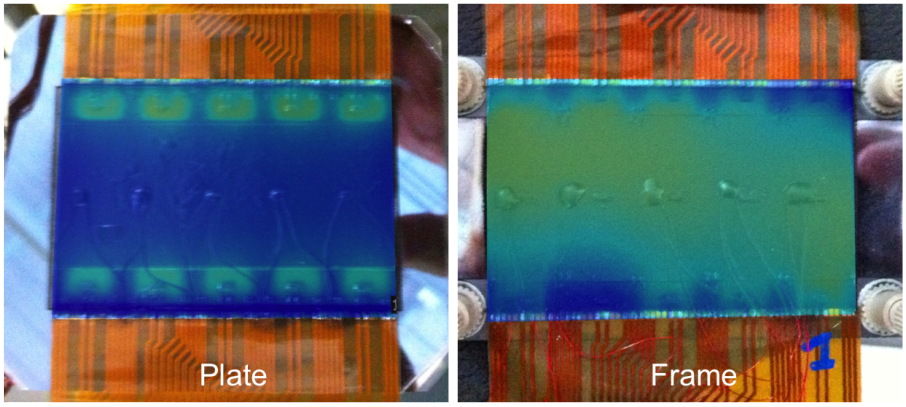


Figure 4.25: Cooling plate and cooling frame with nominal power on silicon mock-ups. Coolant runs with 15 °C inlet temperature.

The power settings in figure 4.26 are worst case scenario power settings. The digital zones dissipate 36 W and the analogue zone dissipates 10 W. The cooling plate keeps the analogue zone at an equal temperature of approximately 10 °C above T_{in} and the digital zones at maximal 20 °C above T_{in}. The cooling frame can keep the analogue zone at approximately 25 °C above T_{in} and the digital zones only slightly cooler. Now the digital zones strongly influence the temperatures in the analogue zones in both examples.

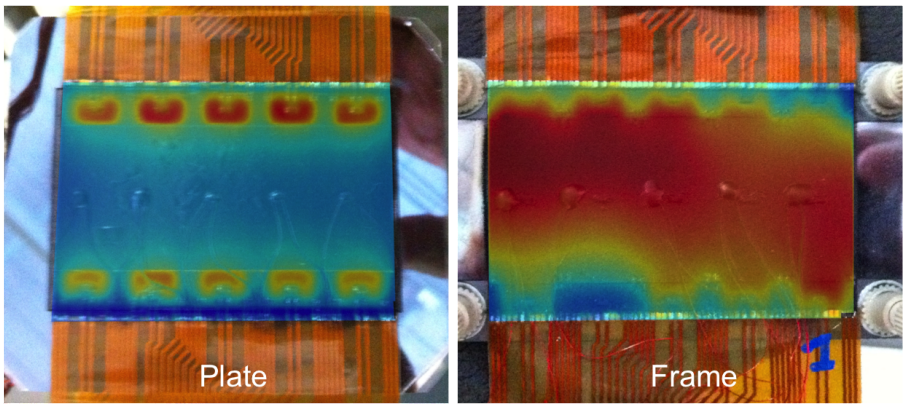


Figure 4.26: Cooling plate and cooling frame with maximal power on silicon mock-ups. Coolant runs with 15 °C inlet temperature.

It is important to mention again, that the high temperatures in the pixel matrix, in case of the cooling frame, are conditional to the concept of the frame. The required temperature can be adjusted with the inlet temperature T_{in}. Figure 4.27 illustrates the thermal behaviour of the 2 concepts and figure 4.28 is a reminder of the two different designs. The cooling plate guarantees an equal thermal behaviour and a cooler temperature to the pixel sensor, but adds material in the sensitive area. In case of the frame, the temperature distribution over the pixel sensor is less uniform and it is warmer, but no material is added in the sensitive area.

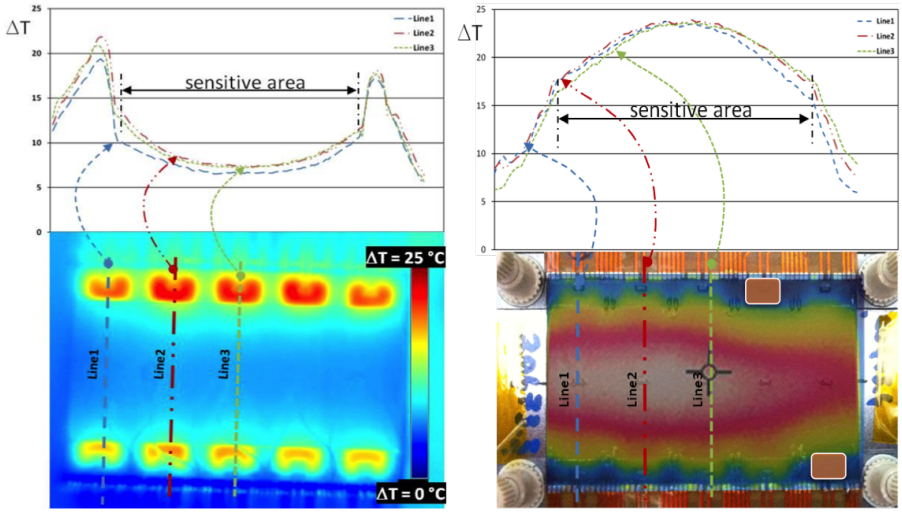


Figure 4.27: Cooling plate and cooling frame with temperature lines over their surface.

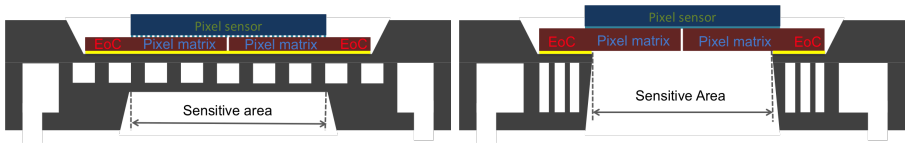


Figure 4.28: Schematics of cooling plate and cooling frame.

Table 4.1: Summary of requirements for the two GTK cooling solutions

Cooling Requirement	Baseline Cooling Plate	Alternative Cooling Frame
stable temperature between 5 and -20 °C	reached the pixel sensor has the lowest temperature; ΔT between coolant and pixel sensor is 5 °C	reached the pixel sensor has the highest temperature; ΔT between coolant and pixel sensor is 15 °C
temperature uniformity on the pixel sensor ±3 °C	very uniform temperature distribution; temperature variation is ±1 °C	less uniform temperature distribution; temperature variation is ±3 °C for the parallel flow and ±2 °C for the counter flow
heat exchanger: max. 150 µm of silicon in the pixel area	130 µm silicon from the cooling plate (pixel sensor 200 µm , ASIC 100 µm)	no extra material added by the heat exchanger, but the ASICs need to be 50 µm to 100 µm thicker
integration aspects	integration concept of cool assembly and PCB works for cooling plate and frame (5.2)	
	mounting of the sensor assembly is more difficult; sensor assembly needs to be very planar	mounting of sensor assembly is easier; frame only touches ASICs on the extremities
costs	higher: large object, difficult geometry (several depths), many production steps, one object per wafer	lower: smaller object, easier geometry (one depths), fewer productions steps, several objects on one wafer
safety	higher hydraulic pressure, around 7 bar	lower hydraulic pressure, around 3.5 bar

Table 4.1 summarizes the results of the cooling performance, the design, the integration and the costs of the two micro channel solutions. It is clearly visible that the thermal performance of the cooling plate outnumbers the one of the cooling frame. The temperature of the pixel area is lower and the temperature distribution is more even. The temperature difference between coolant and pixel sensor is 5 °C for the cooling plate and up to 15 °C for the cooling frame. It means that thermal stress and deformation can be reduced with the cooling plate, but the concept is based on an excellent thermal contact between the cooling plate and all readout chips. If this contact is lost the cooling performance will collapse. The cooling with the cooling frame relies on a much smaller contact surface, which is easier to realize. The higher temperature differences are no problem for the readout chips.

The cooling plate leaves a larger margin for higher power consumption of the readout chips. The cooling performance of the pixel sensor can be kept with a higher mass flow or a slightly bigger temperature difference. The cooling frame will reach its limit already with a slightly higher power consumption of the analogue part of the TDCpix. Since all heat from that part is drained via the cross section of the chip, a higher power consumption of the analogue part leads directly to a bigger temperature difference inside the chip and between coolant and pixel sensor. The temperature uniformity of the cooling plate is better than that of the cooling frame, because it only depends on the temperature uniformity of the coolant running underneath. The temperature difference of the coolant can be regulated with the mass flow. The temperature uniformity of the cooling frame depends again on the power consumption of the analogue part and the cross section of the readout chip, two parameters which can not easily be adapted.

The integration of the cooling frame is easier to realize. It less fragile than the cooling plate. The costs for the cooling plate are higher, since it is more complicated to produce. It needs more micro fabrication steps and more time. In addition, the frame can be produced in larger quantities on one wafer. Finally the cooling frame operates with a lower pressure than the cooling plate and has more material margin. Both aspects lead to more safety during operation.

Outlook

The coolant C_6F_{14} is widely used at CERN and will also cool the NA62 GigaTracKer. The power density of future ASICs for pixel detectors will rise, since the pixel size will decrease and the readout frequency will increase. To cope with these higher cooling demands, one has to take the step from single-phase to two-phase cooling. Two-phase cooling promises smaller a temperature difference between inlet and outlet, since it only depends on the small pressure drop inside the heat exchanger. The necessary mass flow to remove the thermal power will be much smaller, since the latent heat of a cooling fluid is generally much larger than its specific heat capacity.

A very promising coolant for two-phase cooling in HEP is carbon dioxide, CO_2. It has the following relevant qualities:

- radiation hard
- thermally and chemically stable
- non-flammable, non-toxic, non-conducting
- two phase cooling down to -50 °C
- high latent heat, 574 kJ/kg

CO_2 cooling systems have to withstand high pressure. The saturation pressure at 20 °C is 57 bar and at -20 °C it is 20 bar. On the other hand, due to the high latent heat the mass flow can be very small, which means that the piping in CO_2 cooling systems can have very small diameters. Also the return pipes can have a small diameter, since the vapour pressure is still very high and a small pressure drop in the piping is of no consequence. The small pipe diameters mean less material in HEP detectors and therefore fewer unwanted particle interactions.

The development of micro channel heat exchangers for CO_2 had started in parallel with the development of the micro channel frame for the GTK. Both the CMS and the ATLAS detectors foresee the installation of CO_2 cooling systems in their inner detectors in the LHC Long Shutdown 2 (LS2) in 2019. CO_2 micro channel heat exchangers are a good candidate to replace coiling steel tubes as heat exchanger for the inner pixel detectors.

For the NA62 GTK cooling the development of a CO_2 micro channel heat exchanger has already begun. Figure 4.29 shows a micro channel frame stave with micro channels adapted to the coolant CO_2. Also new chip-to-tube solder connections were used for this stave, 5.2.1. The development of the cooling frame offered the possibility to adapt the micro channels to CO_2, because the tight restrictions concerning the material budget do not apply in the frame area. Since a frame can be made thicker than the cooling plate and the channels can be smaller compared to C_6F_{14} channels, the high pressures can be controlled.

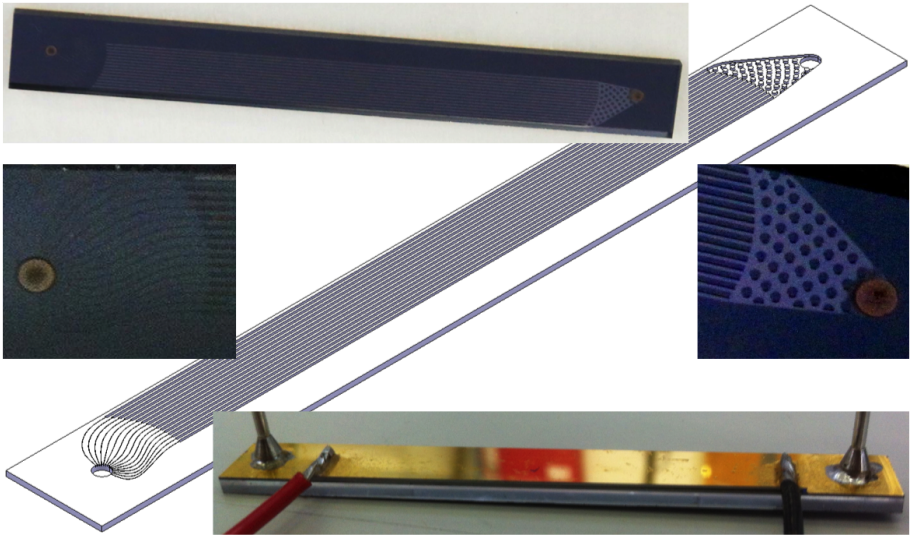


Figure 4.29: Cooling frame stave with micro channels for CO_2 and solder connectors, see 5.2.1.

The object has been successfully tested on a CO_2 cooling plant. Pressures up to 65 bar and temperatures down to -10 °C where reached. The development of a CO_2 cooling frame is ongoing. For the current schedule of the NA62 experiment it will be available to late. In a possible upgrade scenario with higher beam intensity, a CO_2 cooling frame might become an alternative. CO_2 micro channel heat exchangers will be used in HEP, because they introduce less material, are reliable and can easily be adapted to different detector designs.

5 Integration

The chapter presents the ideas and challenges in the assembly of the components of a GTK-module, which can be installed into the Kaon beam line of the NA62 experiment. The aim is to produce a GTK module that can be installed at the 3 positions of the GTK subdetector. The housing for the GTK module is similar at the positions 1 and 2, with the difference that on position 2 the GTK module needs to be 10 mm lower (y-direction) to compensate the beam displacement at this position, see 1.3. At position 3, the GTK module needs to be integrated into the vessel housing the CHANTI subdetector.

5.1 Housing of the GTK modules

The GTK housing in figure 5.1 is made of a cylinder with two KF flanges to connect it to the secondary beam line and two CF blind flanges that guarantee vacuum tightness. One of the two CF blind flanges has an elongated hole to allow the mounting and dismounting of a GTK module, see figure 5.1.

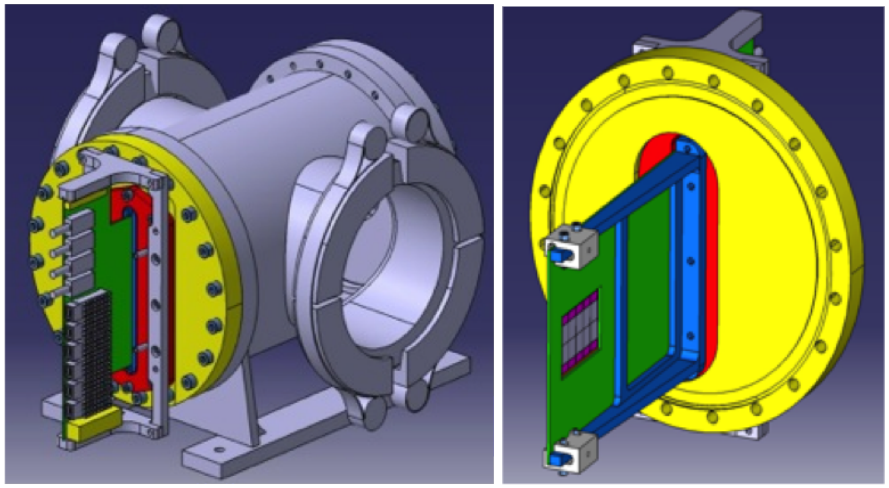


Figure 5.1: GTK housing with installed GTK module and inside view. Courtesy of Nicolas Szilasi, UCL, Belgium

Figure 5.2 shows a prototype of the GTK vessel installed in the NA62 beam line. The vessel was installed on the position of GTK 3 in the technical run in 2012. It was equipped with a holder for a silicon wafer. A silicon wafer was installed to test the influence of the material in the beam. The silicon wafer had a thickness of 380 µm to simulate the influence of GTK 3 on the particle beam.

Figure 5.2: GTK housing installed at the positon of GTK 3 for the technical run in 2012

Figure 5.3 shows a GTK module integrated into the CHANTI vessel. The GTK module for position 3 does not differ from those of positions 1 and 2. The modules can be mounted on all 3 positions.

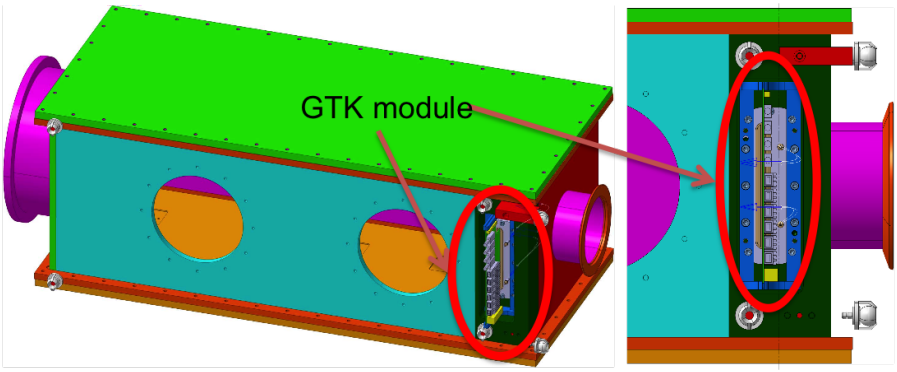


Figure 5.3: GTK module at position 3 integrated into the CHANTI vessel. Courtesy of the CHANTI subdetector group

5.2 GTK Module Assembly

The GTK module consists of the following parts

- the sensor assembly, composed of the silicon pixel sensor and 10 bump bonded readout chips, TDCpix, underneath, figure 5.4
- the mc heat exchanger, cooling plate or cooling frame with its connections, figure 5.5
- the PCB, printed circuit board with its electronic components, figure 5.6
- the flange that guarantees vacuum tightness and positioning of the GTK module relative to the housing and the beam, figure 5.7

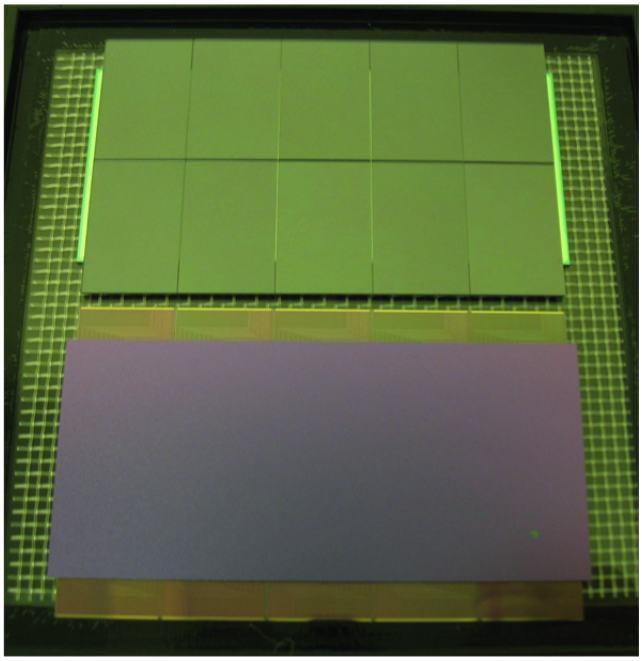


Figure 5.4: Sensor assembly dummy, used to verify the bump bonding process. Courtesy of Massimiliano Fiorini, INFN Ferrara, Italy

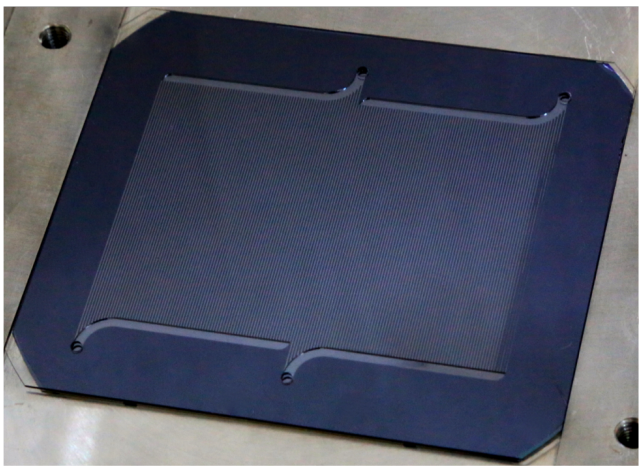


Figure 5.5: Baseline micro channel cooling plate.

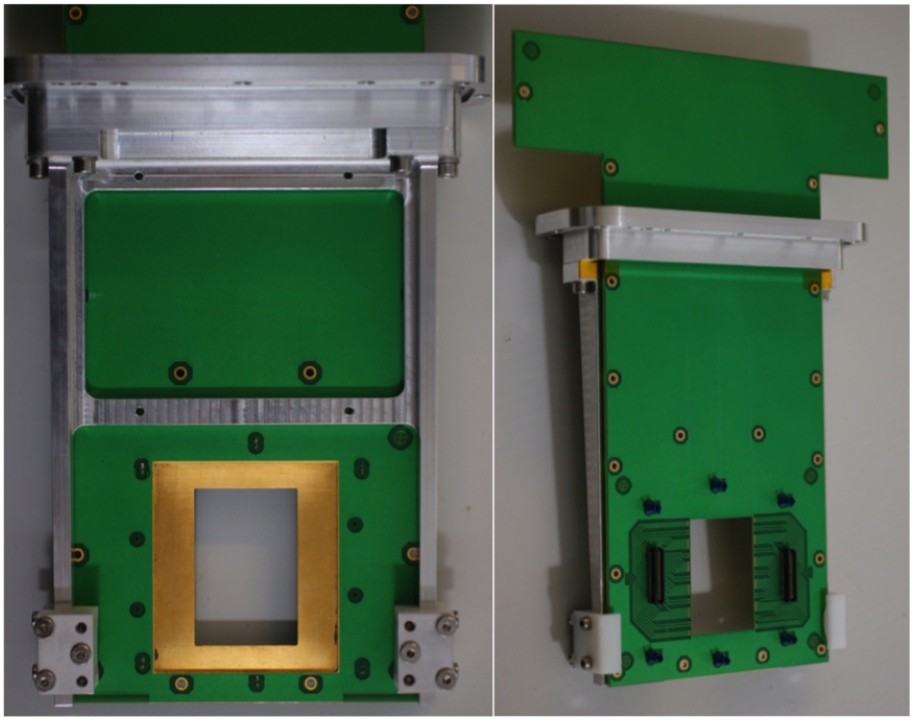


Figure 5.6: Printed circuit board, front and back. Flange and support are mounted for trials.

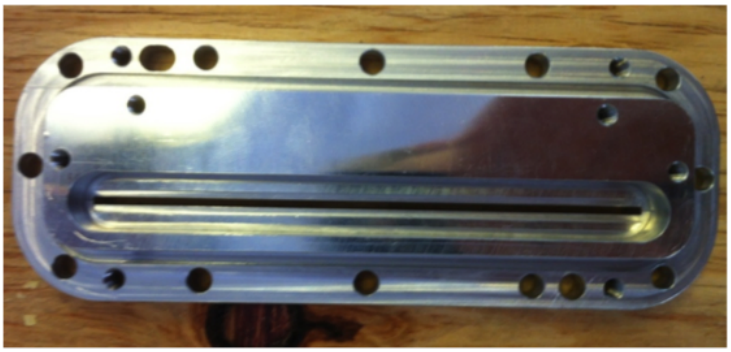


Figure 5.7: Flange for repeatable geometrical precision during installation.

The sensor assembly, described in 1.3, needs to be mounted on the cooling plate or frame. The connection between the two components guarantees a

good thermal connection. Gluing with thin film glue is the chosen technique, [69]. The combination of sensor assembly and coolling plate, cool assembly then needs to be mounted in the PCB. Glue in one corner and clips will hold it in position. At this stage the wire bonding between readout chips and PCB is performed, see figure 5.8.

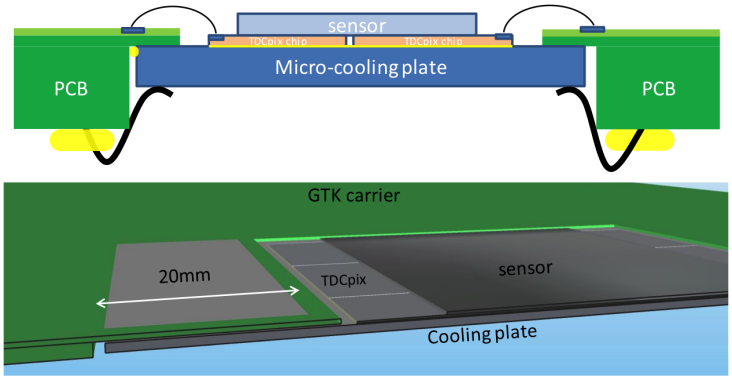


Figure 5.8: The cool assembly inside the PCB, where the TDCpix is wire bonded to the PCB. Courtesy of Michel Morel, CERN, Switzerland

The flange is then glued onto the PCB. The vacuum tightness is ensured by filling the PCB feed through with a liquid epoxy glue, like Araldite 2020, which will go into the smallest cavities. The flange has an O-ring seal for vacuum tightness to the GTK vessel. The resulting GTK module can then be installed into the different vessels on all three positions of the GTK subdetector. Figure 5.9 shows a complete GTK module in a CF flange.

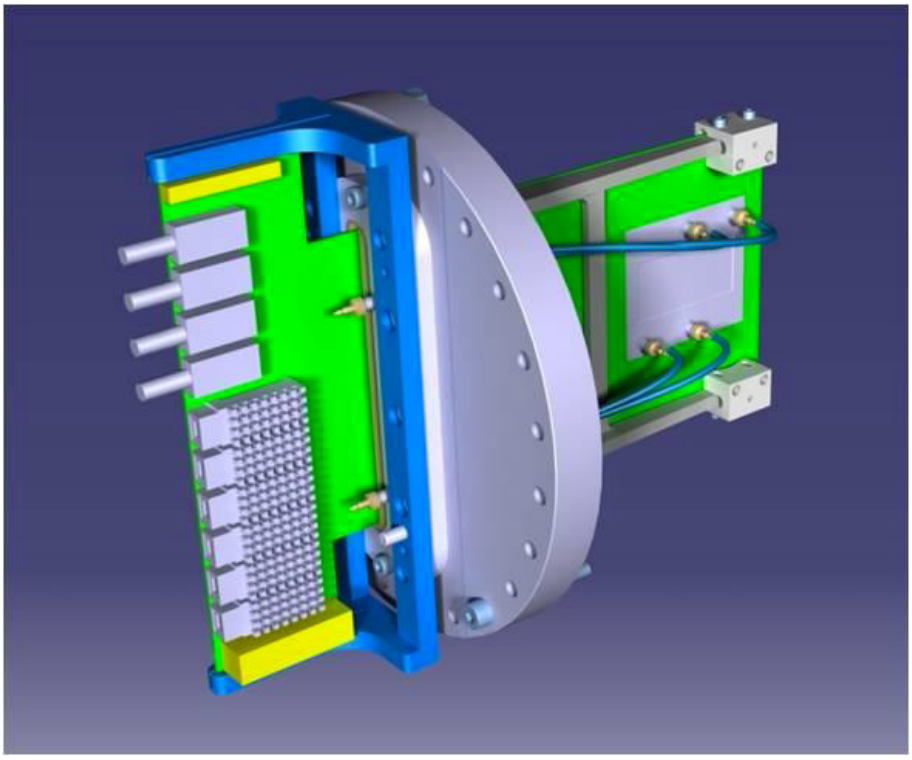


Figure 5.9: The cool assembly inside the PCB, where the TDCpix is wire bonded to the PCB. Courtesy of Nicolas Szilasi, UCL, Belgium

For the production of the GTK modules with precise positioning and repeatability, several jigs are necessary. The first jig is needed to glue the sensor assembly onto the cooling plate, see figure 5.10. Here geometric positioning is not of extreme importance. The geometric position is guaranteed in the next step, when the cool assembly is mounted onto the PCB. Here one has to align the wire bonding pads on the ASICs and on the PCB relative to each other. This guarantees the positioning of the pixel sensor inside the PCB.

The positioning information is then transferred to the flange, figure 5.7. The PCB and flange have to be aligned very precisely to each other and then glued together. The flange itself has two hole for guiding pins on its circumference. This hole/pin combination gives the positioning information of the pixel sensor to the outside of the vessel. The outside of the vessel has fiducial marks, which

allow the correct positioning of the GTK vessels to each other. The alignment of the three GTK stations is done with GTK 3 as a fix point. Since it is located inside the CHANTI vessel, it cannot be moved easily.

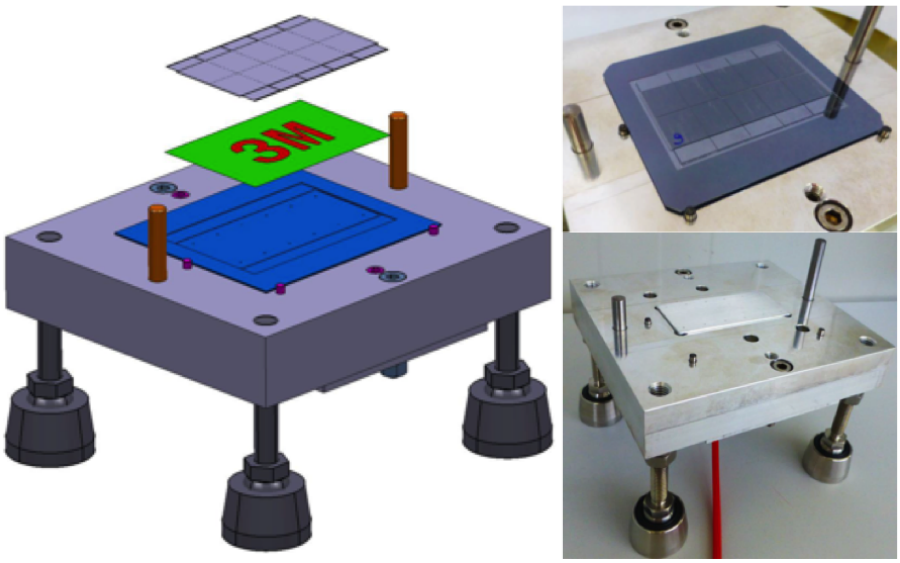


Figure 5.10: The concept of jig 1 includes guiding pins and fixation with vacuum for the different alignment steps. The right side shows a first gluing trial with mechanical dummys. Courtesy of the PH-DT group, CERN, Switzerland

Jig 2 will be a jig that combines several functionalities:

- precise mounting of the cool assembly into the PCB,
- support for the wire bonding between ASICs and PCB,
- precise gluing between PCB and flange.

Ideally, the first step to be performed is the gluing between the PCB and the flange. A precise positioning can be achieved by using the bonding pads on the PCB, the guiding holes in the flange and the inner surface of the flange (in touch with the CF flange) as reference marks. After that the positioning of the cool assembly inside the PCB is done by the bonding pads on each side. Once the cool assembly is fixed inside the PCB the wire bonding can be performed.

Here the jig has to give support to the cool assembly and the ASICs. During wire bonding the cool assembly cannot move.

Several proposals for the jig are under discussion. Most promising is the positioning of the cool assembly with micrometer screws and a piston that fixes the cool assembly with vacuum. The piston can be precisely moved in x-, y- and z-direction.

5.2.1 Solder Connections

The use of Nanoport connectors in the final assembly is excluded. The glue connection to the silicon surface is not reliable in long term use. Additionally the glue seems to weaken with humidity and its behaviour under radiation is questionable. For test purposes the Nanoport connectors were useful, due to easy mounting and dismounting feature. A break of a connector during a beam run would have serious consequences. The secondary beam vacuum would be destroyed and surfaces in the whole detector would be polluted. Therefore a non detachable solution has to be found.

Edward R. Murphy describes the soldering and desoldering of metallic tubes on to gold coated silicon surfaces for lab-on-a-chip devices used in biochemistry [58]. The method is based on the use of stainless steel tubes and Swagelok fittings [73], see figure 5.11. To create a solder-able surface at the end of a tube on has to use a brass back ferrule and the mounting direction towards the end of the tube is reversed compared to the normal use of Swagelok fittings, see figure 5.12. While the ferrules are tightened, they cut into the pipe and create a non-reversible and leak tight connection. The soldering only takes place between the brass back ferrule and the coated silicon surface.

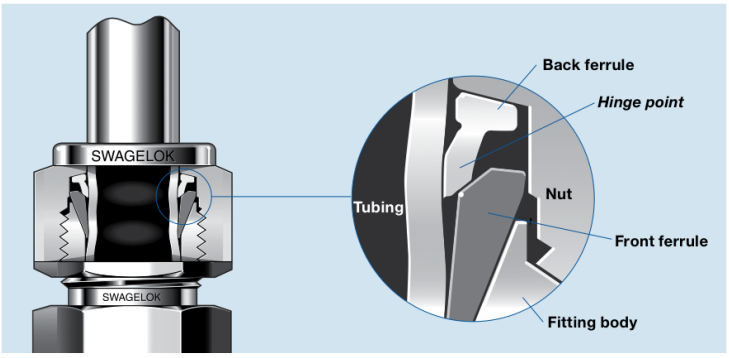


Figure 5.11: The principle of the Swagelok fitting connector [73].

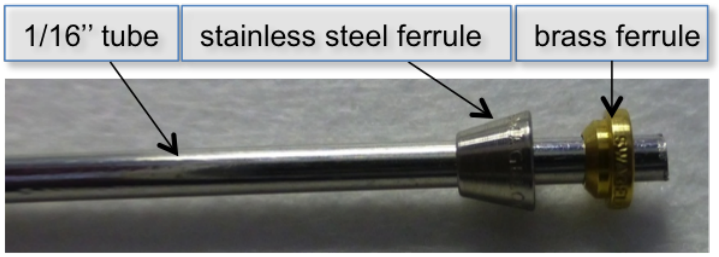


Figure 5.12: The Swagelok ferrules are uses to create a solder-able surface.

In a first trial a stainless steel tube was soldered on a 100 µm thick silicon piece, coated with 20 nm titanium and 200 nm gold, see figure 5.13. In a pressure test with water, the silicon ruptured at a pressure of 37 bar. The solder connection stayed unharmed and tight. It is visible that the tube was not blocked by tin-solder, since it does not wet stainless steel. The microscopic analysis in figure 5.14 confirms that tin-solder only connects the coated silicon surface and the brass back ferrule.

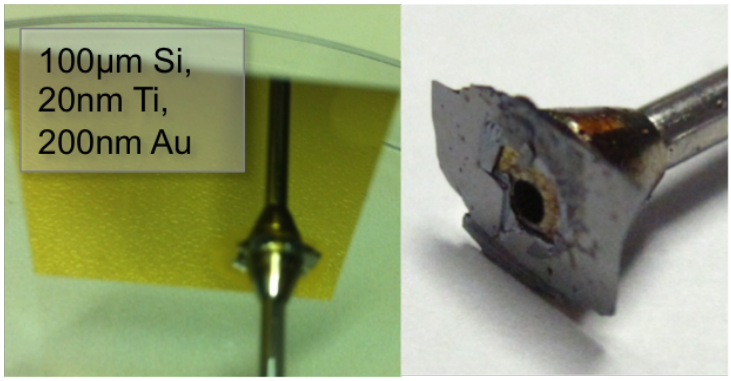


Figure 5.13: A first soldering trial on a 100 µm thick silicon piece. The silicon ruptured at 37 bar water pressure.

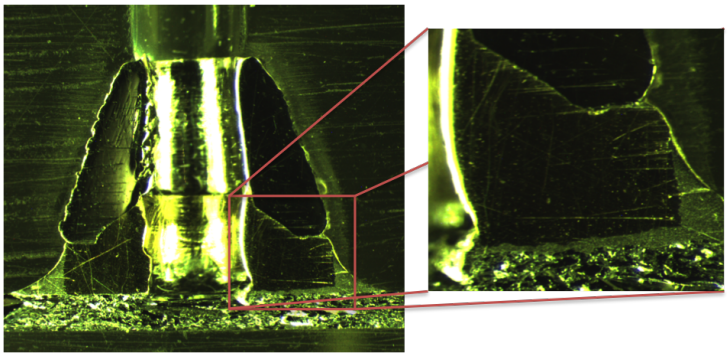


Figure 5.14: Cut of a soldering connection under the microscope. The stainless steel tube is missing, since it was destroyed during the preparation of the cut.

The second trial aimed to prove that flow through these connections is possible. Figure 5.15 shows a micro channel heat exchanger for the ATLAS inner detector with tubes soldered to inlet and outlet. A simple heater was glued on top of the heat exchanger to prove that heat is transferred to a fluid flow. A stable temperature on the surface of the heater indicates that the heat is transported away by a flow. The object was tested on CO_2 two-phase cooling plant up to a pressure of 65 bar. Figure 5.16 shows the results of this test. The thermal picture shows a stable surface temperatures at an electric power of 36 W. Due to the very effective heat transfer of two-phase flow, the electric power had to

be very high in order to create a temperature difference on the surface of the heater.

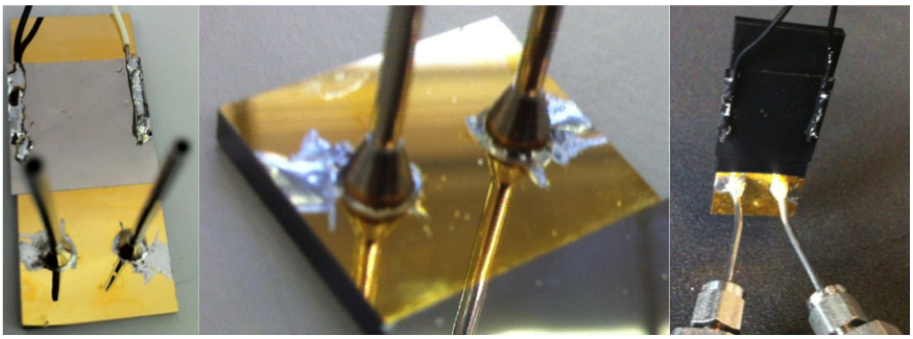


Figure 5.15: Two tubes soldered on to a mc heat exchanger for ATLAS inner detector.

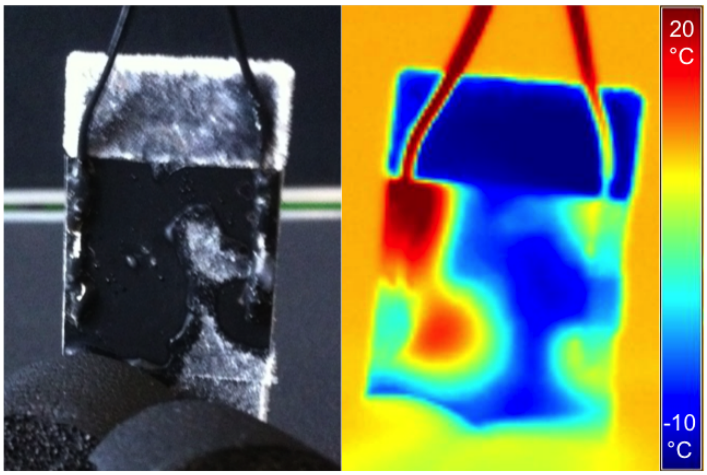


Figure 5.16: Test on a CO_2 cooling plant with an electric power of 36 W.

The very promising results of the above mentioned trials lead to the decision to use this technology to connect the baseline cooling plate and the cooling frame to its tubing, see figure 5.17.

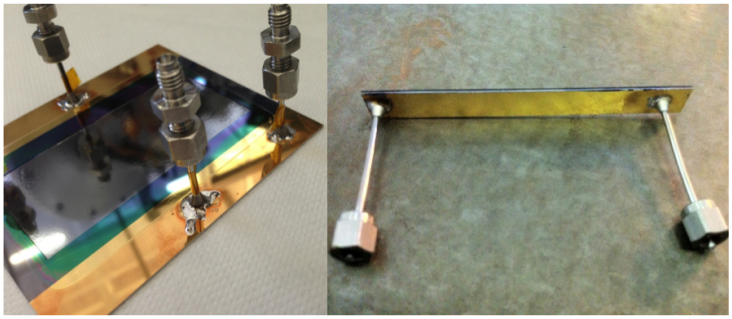


Figure 5.17: GTK baseline cooling plate and cooling frame stave equipped with solder connections.

Both objects were hydraulically tested in the mc test stand at low temperature and under vacuum, see figure 5.18. The objects underwent thermal cycling as well. The baseline cooling plate was also equipped with silicon dummy electronics. The hydraulic and thermal results were comparable to the results achieved with the Nanoport connectors. The silicon dummy electronics had a bad thermal contact to the cooling plate. The resulting temperatures could not show the real cooling capacity of the cooling plate.

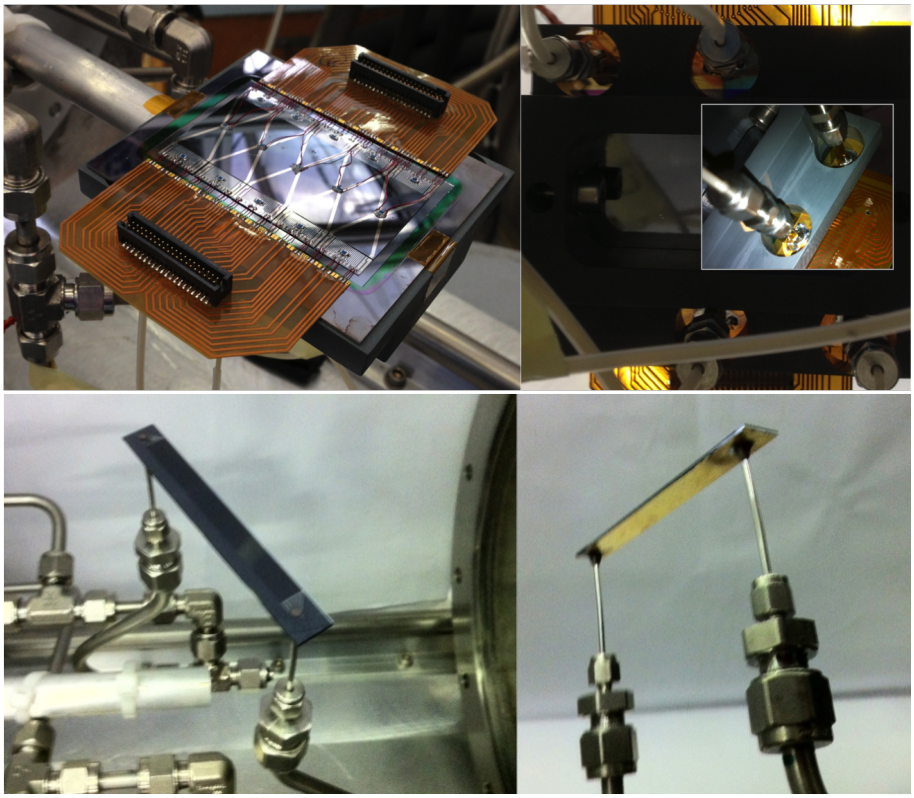


Figure 5.18: Plate and frame stave installed in the mc test stand for hydraulic and thermal test.

With the above described work the concept of soldering tubes to the surface of micro channel cooling devices could be proven. The connections are leak tight, withstand thermal cycling, work down to -25 °C and withstand high pressure. In fact, a few connection samples underwent pressure tests up to 150 bar without breaking. A critical point is to find the right combination of materials that need to be sputtered on the silicon surface in order to create a solderable surface. Here a combination of first titanium and second gold showed great potential. Soldering onto glass surfaces has also been tried, but a good combination of materials has not yet been found.

Soldering tubes to micro channel cooling devices will become a standard solution in HEP. The connections need to be very reliable in radioactive environ-

ments and in vacuum. Additionally the connections are typically in inaccessible places and need to be have a long life time. Adapted connectors that can be soldered to silicon surfaces are under development for the final installation of the GTK detector. Here, specially machined pieces are welded to the end of a tube to create a solder-able surface. The solution to use commercially available ferrules from Swagelok has the charm that it can be produced with simple tools available in most workshops. In laboratories it will be further in use, to test micro channel silicon devices.

6 Summary and Outlook

6.1 Summary

This work started as a study of feasibility to use the novel technique of silicon micro channel heat exchangers for cooling in HEP. Thereby it has been demonstrated that the use of micro channels embedded in silicon wafers, as low material budget heat exchangers, enhances the cooling performance for HEP semiconductor pixel detectors. The main benefits for HEP applications that have been achieved are a very low material budget, an even temperature distribution, a liquid cooling in vacuum and a high adaptability to the cooling needs. Cooling solutions with pipes and high thermally conductive carbon plates can not reach the same level of uniformity, since the cold source is located in one line underneath or next to the heat source. The heat needs to be conducted from its point of origin to the cold source through a carrier material.

Cooling plate and frame

The NA62 experiment was the first HEP experiment to consider silicon micro channel heat exchangers for cooling. In particular two solutions have been developed for the NA62 GTK detector, the so called baseline or plate solution and the alternative or frame solution. Both solutions fulfil the requirements of the GTK detector, namely an operating temperature of 5 °C or lower, a temperature difference between inlet and outlet of 5 °C, a temperature spread of ±3 °C over the pixel sensor, a material budget of 150 µm silicon or less and an operation in vacuum. Both concepts have specific advantages and shortcomings.

Thermal behaviour The cooling plate cools the pixel area to a lower temperature than the cooling frame and its temperature distribution is more even compared to the cooling frame (4.1.2,4.2.2). The temperature difference between coolant and pixel sensor is 5 °C for the cooling plate and up to 15 °C for the cooling frame. It means that thermal stress and deformation can be reduced with the cooling plate. The concept is based on an excellent thermal contact between the cooling plate and all readout chips over the total of the chip surface. The cooling plate leaves a larger margin for a rising power consumption of the readout chips (4.3). The cooling frame relies on a much smaller contact surface, which is easier to realize. Therefore the temperature differences are higher compared to the cooling plate, but high temperatures are no problem for readout chips. Conventional cooling solutions, using pipes and high-conductive carbon plates, see much larger temperature differences between coolant and pixel sensor. In the best case the temperature difference is around 14 °C, but it can rise to more than 25 °C.

Material budget The low material budget needed for micro channel cooling plate and frame is one of the key advantages compared to conventional cooling solutions with pipes. It is fair to compare the concept of the cooling frame (3.2) to cooling with pipes. One cooling pipe adds about 10 times the material needed for a cooling frame underneath a readout chip. Although the area of the added material is very small (pipe diameter times pipe length), the pipe needs to be thermally connected to a heat conducting layer that drains the heat from the readout chips and conducts it to the cooling pipe. This layer also adds to the total material budget and is comparable to the thickness of a cooling frame. The frame adds no material in the sensitive area underneath the pixel sensor, but relies on the thermal conduction inside the readout chip. The material budget of the cooling plate is comparable to the one of the frame (3.1). The cooling plate adds about the same amount of material in the sensitive region as thicker readout chips in the frame concept, which are needed to conduct the heat to the extremities of the readout chip.

Production and costs The broader range in cooling capacity speaks for the cooling plate, but its integration might become more difficult. The cooling frame has its advantages in the absence of extra material in the sensitive area under the pixel sensor and an easier integration. The integration of the cooling frame is easier to realize, since it is less fragile than the cooling plate. The costs for the cooling plate are higher, since its production is more complicated. The cooling plate needs multiple micro fabrication steps in its production and it has higher requirements on planarity, therefore it is more time consuming. Instead, the frame can be produced in larger quantities on one wafer. Finally the cooling frame operates with a lower pressure than the cooling plate and does not add extra material in beam area. Both aspects lead to more safety during operation. The micro channel cooling plate was chosen as the baseline cooling solution for the NA62 GTK, since it guarantees a lower and more stable temperature for the pixel sensor and can deal with higher heat flux densities.

Micro channel layout and production

The thermo-hydraulic layout of the micro channels was realized with a purely analytic approach. For the hydraulic layout of micro channels and embedded manifolds, it was necessary to model the geometry and simulate the flow conditions. It was shown that CFD simulations predict very accurately the pressure drop and the flow distribution of the coolant. With these methods multiple geometry variations (table 3.2) could be studied during the design process, without the need to produce prototypes. The prototype production was realized at the EPFL clean room in Lausanne, according to the layout resulting from the design process. A first production of 10 final heat exchanger was outsourced to an external company. The quality of the received products was only partially satisfactory. Nevertheless, the heat exchangers were successfully installed in the NA62 beamline, see figure 6.1.

Coolant and Testing

The coolant C_6F_{14}, Perfluorohexane, was chosen for its radiation hardness, excellent electrical insulation and the good and long experience with it at CERN

(3). The use of other coolants, like demineralized water and carbon dioxide, was considered, but rejected due to the high radiation and the complexity of two-phase cooling circuits. A test stand, operated with C_6F_{14}, for tests in ambient atmosphere and in vacuum has been designed, build and commissioned. The test stand can also be run with other coolants if needed. The data acquisition reads and saves the data from 18 temperature probes, a mass flow meter, two pressure probes and two power supplies. Test procedures and data analysis has been developed and implemented. The equipment and the test procedures are in use to qualify the heat sinks that will be installed in the experiment. In the future, the whole installation will be of use in the development of other micro channel heat sinks for pixel sensors. Thermal imaging has been introduced as a second line of testing to visualize and evaluate the cooling capacity of micro channel heat sinks (4.3). The quality of the thermal imaging has been greatly improved treating the surfaces of mock-up electronic and heat sinks. The images are of great use in the investigation of the cooling capacity of future heat sinks.

Electronic mock-ups and chip-to-tube solder connections

During the development of the micro channel heat sink for the GTK, it became obvious that highly sophisticated mock-up electronics are necessary to evaluate the performance of the cooling concepts. This opened a new line of development (3.4.1). The electronic mock-ups are made from silicon, like the readout chips, and have the same geometric features as the final readout chips. For the NA62 GTK micro channel cooling two different zones of power density of the readout chips are represented on the electronic mock-ups with two independent resistors covering the two areas accordingly. These dedicated electronic mock-ups are necessary in future cooling developments in HEP to cope with higher and uneven heat flux densities, less material and cooling in vacuum.

An integration strategy was developed and its realization started with my participation and is continued by the PH-DT-group. The problem of connecting micro channel heat sinks to a cooling circuit has been solved with the adaptation and the successful testing of the chip-to-tube soldering (5.2.1). Pressures of more than 100 bar were reached without any damage. Previously used connectors only reached maximal 20 bar. The solder connections were successfully

tested in a CO_2 two-phase cooling circuit up to 70 bar. This technique provides safety and reliability and will become a standard for the connection of silicon micro channel heat exchangers with its piping for the use in HEP. Furthermore, applications outside HEP, which use micro channel heat exchangers, should adopt this solution.

6.2 Outlook

The NA62 experiment choose the micro channel baseline cooling plate option over the gas cooling option for the cooling of the GTK pixel detector [61]. The final NA62 GTK module can be seen in figure 6.1, as installed in the beam in October 2014. The final module was produced by the PH-DT-group in collaboration with the PH-ESE-group. Pipes from the liquid feedthrough of the flange to the flow split for inlet and outlet, as well as to the solder connections on the cooling plate (right side) are visible in figure 6.1. The pipe routing has been adapted to compensate for contraction and expansion during operation. It minimizes the mechanical stress transferred from the solder connections to the silicon micro channel cooling plate.

The NA62 GTK is the first detector in HEP that uses a micro channel heat sink to cool its detector. In the future other experiments will adapt this solution. The LHCb experiment strongly investigates the use of micro channel cooling in their VELO detector [68]. The VELO detector will operate in vacuum and has a low material budget. For this application the micro channel heat sink has to cool a non-rectangular surface and the micro channels can not run in a straight line but instead they must follow the shape of the detector. Also the ATLAS experiment considers the use of micro channel cooling for their IBL detector upgrade. Both detectors will use CO_2 two-phase cooling for their detectors.

In the the ALICE experiment micro channel cooling frames are a candidate for the update of their vertex detector [37]. The ALICE vertex detector uses a two-phase cooling with C_4F_{10}. The plan is to replace the conventional cooling pipes under the readout chips with micro channel heat sinks, in which the cooling fluid runs.

Outside HEP micro channel cooling is used to directly cool the CPU (Central

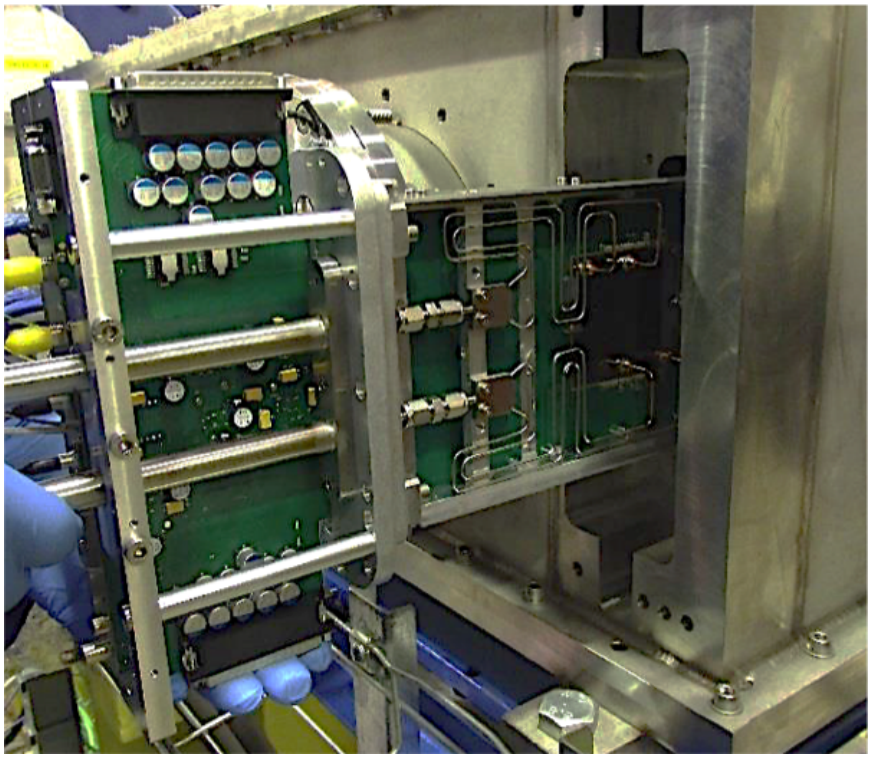


Figure 6.1: The first GTK module before insertion into the vessel on the GTK3-position [28].

Processing Unit) and other components in blade computers of data centres. This application triggered the investigation of using micro channel cooling in HEP [78]. Material thickness, radiation and vacuum are no issues for this application. The coolant is normally de-mineralised water. Here the challenge is the tight packing of modern server farms. Conventional cooling via a cold air stream is not efficient any more, therefore liquid cooling is a good alternative, since it provides a reliable and stable temperature. Additionally, the heat in the cooling water can be of use in downstream processes.

Another application of microfluidic channels is gas chromatography [66]. Here micro channels are used in MEMS (Micro ElectroMechanical Systems) to analyse gases. In contrary to HEP cooling applications, mass flow rate, material thickness and radiation are of little interest. In the same category are Lab-on-a-chip applications, which are widely used in biology and chemistry [58]. Their

purpose is mostly to bring a solid in contact with a liquid to trigger a reaction.

The producible size of silicon micro channel heat exchangers for cooling in HEP is momentarily limited by the available silicon wafer diameter. A next step to overcome this limit is the investigation of micro channel interconnections. The CERN PH-DT group explores these possibilities and first promising results have been achieved and presented [37]. If one thinks two steps ahead, the ideal cooling solution would be the integration of micro channels into the readout chip production. Here one could imagine that a wafer containing the micro channels is bonded to a wafer that will host the readout chips. The proper alignment between micro channels and the photolithography of the electronics will be crucial for this production. This bonded wafer can then be used as a normal wafer in the production of the readout chips. In this way the readout chips would be ideally thermally connected to a cooling fluid. Such a device could deal with very high heat fluxes and would still remain at a low and even temperature.

A last point to look at for the improvement of detector cooling is the choice of a coolant. Undoubtedly, the two-phase coolant CO_2 will be the future for cooling in HEP. The small temperature differences and the small necessary mass flows are key features for this coolant. Additionally it will improve the uniformity of the temperature distribution. The rising power of ASICs, the lower material budgets for cooling and the lower temperatures needed to keep silicon sensors from rapid ageing under radiation, force the development of CO_2 cooling plants and heat exchangers. High pressures are intrinsic for cooling with CO_2. Micro channel heat sinks can easily cope with this high pressures, due to their small dimensions (4.3). Therefore they are predestined to be used as heat exchangers in CO_2 cooling circuits.

One important limitation of micro channels is their usable length. Given the small dimensions of micro channel cross sections, long micro channels produce a high pressure drop. The high ratio between perimeters and cross sections of a micro channel array causes plenty of interaction and friction of the coolant with walls. This is favourable for heat transfer, but unfavourable for the overall pressure drop. As a consequence micro channel heat sinks can be used for direct

cooling of detector modules in the cm range. Each heat sink has to be connected to a piping network to distribute the coolant.

The work elucidates the scientific and practical fundamentals used in the design, layout and testing of silicon micro channel heat exchangers for liquid coolants. The design of the micro channel heat sinks can easily be adapted to the cooling needs of detectors and to single- and two-phase coolants. The work demonstrates that, together with chip-to-tube soldering, micro channel heat sinks are an excellent candidate for the local thermal management of silicon pixel detectors in High Energy Physics applications.

This work started from scratch with the idea to adapt micro channel cooling to the needs of HEP detectors. Its results have been presented at IRPD 2010 [54], in the Journal of Instrumentation 2012 [55], in the Microelectronics Journal 2013 [62], at ICATPP 2013 [61] and on a regular basis in the NA62 GTK working group meetings [12].

Bibliography

[1] http://cmi.epfl.ch/, October 2014.

[2] http://cp3.irmp.ucl.ac.be/, November 2014.

[3] http://na62.web.cern.ch, October 2014.

[4] http://ph-dep-dt.web.cern.ch/, November 2014.

[5] http://ph-dep-ese.web.cern.ch/ph-dep-ese/, November 2014.

[6] http://switzerland.ni.com/, November 2014.

[7] http://www.idex-hs.com/product-families/3/fittings-upchurch-scientific-rheodyne-isolation-technologies.aspx, March 2014.

[8] http://www.minco.com, November 2014.

[9] http://www.samtec.com/, November 2014.

[10] http://en.wikipedia.org/wiki/cp_violation, February 2015.

[11] http://home.web.cern.ch/, May 2015.

[12] http://indico.cern.ch/category/2306/, September 2015.

[13] http://www.matweb.com/, May 2015.

[14] 3M. *3M Fluorinert, Electronic Liquid FC-72*. 3M Specialty Materials, 3M Center, Building 223-6S-04, St. Paus, MN, 55144-1000, May 2000.

[15] A. Abashian et al. *The Belle detector*, volume A. Nuclear Instruments and Methods in Physics Research, 2002.

[16] J. K. Ahn et al. Experimental study of the decay $K_L^0 \to \pi^0 \nu\bar{\nu}$. *Phys. Rev.*, D81:072004, 2010.

[17] A.Kluge. The TDCpix readout ASIC: A 75 ps resolution timing front-end for the NA62 Gigatracker hybrid pixel detector. In *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, volume 732, pages 511–514. Vienna Conference on Instumentation, ELSEVIER, 2013.

[18] Wolfgang Altmannshofer, Andrzej J. Buras, Stefania Gori, Paride Paradisi, and David M. Straub. Anatomy and Phenomenology of FCNC and CPV Effects in SUSY Theories. *Nucl. Phys.*, B830:17–94, 2010.

[19] A.V. Artamonov et al. New measurement of the $K^+ \to \pi^+\nu\bar{\nu}$ branching ratio. *Phys.Rev.Lett. 101(2008)191802*, 2008.

[20] Monika Blanke, Andrzej J. Buras, Bjorn Duling, Katrin Gemmler, and Stefania Gori. Rare K and B Decays in a Warped Extra Dimension with Custodial Protection. *JHEP*, 03:108, 2009.

[21] Monika Blanke, Andrzej J. Buras, Bjorn Duling, Stefan Recksiegel, and Cecilia Tarantino. FCNC Processes in the Littlest Higgs Model with T-Parity: a 2009 Look. *Acta Phys. Polon.*, B41:657–683, 2010.

[22] Joachim Brod, Martin Gorbahn, and Emmanuel Stamou. Two-Loop Electroweak Corrections for the $K- > \pi\nu\bar{\nu}$ Decays. *Phys. Rev.*, D83:034030, February 2011.

[23] H. Bruus. *Theoretical Microfluidics*. Oxford University Press, 2008.

[24] A. J. Buras et al. The rare $K^+ \to \pi^+\nu\overline{\nu}$ at the next-to-leading order in QCD. *Phys.Rev.Lett. 95(2005)261805*, 2005.

[25] Andrzej J. Buras, Dario Buttazzo, Jennifer Girrbach-Noe, and Robert Knegjens. $K^+ \to \pi^+\nu\bar{\nu}$ and $K_L \to \pi^0\nu\bar{\nu}$ in the Standard Model: Status and Perspectives. 2015.

[26] Andrzej J. Buras, Fulvia De Fazio, and Jennifer Girrbach. The Anatomy of Z' and Z with Flavour Changing Neutral Currents in the Flavour Precision Era. *JHEP*, 02:116, 2013.

[27] A. Ceccucci et al. *Proposal to Measure the Rare Decay $K^+ \to \pi^+\nu\overline{\nu}$ at the CERN SPS*. June 2005.

[28] A. Ceccucci et al. NA62 @ FRC4. Finance Review Committe 4th meeting, 2014.

[29] Jorgen Christiansen. Electronics for HL-LHC trackers. In *ECFA*, 2013.

[30] CMS-collaboration. *The CMS experiment at the CERN LHC*, volume 3 S08004. The CMS collaboration, 2008.

[31] The BaBar Collaboration. *The BaBar Detector*, volume A, pages 1–116. Nuclear Instruments and Methods in Physics Research, 2002.

[32] E. Da Riva et al. EN Cooling and Ventilation, Activity report on NA62-GTK project. September 2011.

[33] M. D'Alfonso et al. Validation tests of the CMS TIB/TID structures. Technical Report 2009/010, CMS Note, 2009.

[34] DELPHI Collaboration. The Delphi Detector at LEP. *Nuclear Instruments and Methods in Physics Research*, 1990.

[35] eFunda Inc. efunda, May 2013.

[36] W. Escher et al. *Experimental Investigation of an Ultrathin Manifold Microchannel Heat Sink for Liquid-Cooled Chips*, volume 132. International Journal of Heat and Fluit Flow, August 2010.

[37] A. Francescon et al. Development of interconnected silicon microevaporators for the on-detector electronics cooling of the future ITS detector in the ALICE experiment at LHC. 4th Micro and Nano Flows Conference, London, UK, 2014.

[38] E. Goudzovski. Kaon experiments at cern: recent results and prospects, Aug. 2012.

[39] H. Gröber and S. Erk. *Die Grundgesetze der Wärmeübertragung*. Springer-Verlag, 3rd edition, 1955.

[40] J. F. Große-Oetringhaus. Zerfall neutraler Kaonen und CP-Verletzung. 2009.

[41] F. Hartmann. *Evolution of Silicon Sensor Technology in Particle Physics*. Springer, Berlin, 2009.

[42] F. Hartmann. Silicon tracking detectors in high-energy physics. *Nuclear Instruments and Methods in Physics Research*, A(666):25–46, 2012.

[43] P. Hobson. Silicon tracking detectors for hep, 2009.

[44] R. Horisberger. CMS Pixel Issues. ACES 07, Common ATLAS — CMS Electronics Workshop, March 2007.

[45] S. Ilie et al. Chemical and radiolytical characterization of perflourocarbon fluids used as coolant for the lhc experiments, 2007. TS-Note-2007-005, EDMS Nr: 842110.

[46] F. Incropera et al. *Principles of Heat and Mass Transfer*. John Whiley and Sons, 7th edition, 2013.

[47] H. Jungnickel, R. Agsten, and E. Kraus. *Grundlagen der Kältetechnik*. VEB Verlag Technik Berlin, 2nd edition, 1985.

[48] T.K. Komatsubara. Experiments with K-Meson Decays. *Prog.Part.Nucl.Phys.*, 67:995–1018, 2012.

[49] Krohne. *OPTIMASS 3000 Technical Datasheet*, November 2013.

[50] Z. Li. Radiation hardness/tolerance of si sensors detectors for nuclear and high energy physics experiments. In *Proc. PIXEL Int. Workshop, Carmel, CA*. Proc. PIXEL Int. Workshop, Carmel, CA, 2002.

[51] Y. Madour et al. *Flow Boiling of R134a in a Multi-Microchannel Heat Sink with Hotspot Heaters for Energy-Efficient Microelectronic CPU Cooling Applications*, volume 1. IEEE Trans. on Components, Packaging and Manufacturing Technology, 2011.

[52] Luciano Maiani. The GIM Mechanism: origin, predictions and recent uses. La Thuile, Valle d'Aosta, Italy, March 2013. Rencontre de Moriond, EW Interactions and Unified Theories.

[53] Marcello Mannelli. CMS Tracking Trigger Strawmen. In *CERN ACES Workshop*, February 2009.

[54] A. Mapelli et al. Low material budget microfabricated cooling devices for particle detectors and front-end electronics. In *Innovative Particle and Radiation Detectors, IPRD10*, 2010.

[55] A. Mapelli et al. *Microfluidic Cooling for Detectors and Electronics*, volume 7, C01111. J. Instr., 2012.

[56] F. Marchetto et al. GTK cooling specifications. October 2011.

[57] MatWeb. Matweb, May 2013.

[58] E. R. Murphy et al. Solder-based chip-to-tube and chip-to-chip packaging for microfluidic devices. *Lab Chip*, 7:1309–1314, July 2007.

[59] NA62-Collaboration. Na62 technical design document. Technical report, 2010.

[60] I. Newton. *Phil. Trans. roy. Soc. (London) 22*, page 824, 1701.

[61] G. Nüßle. NA62 GigaTracKer Cooling with Micro Channels. ICATPP, World Scientific, 2013.

[62] P. Petagna et al. *Application of Micro-channel Cooling to the Local Thermal Management of Detectors Electronics for Particle Physics*, volume 44, pages 612–618. Microelectronics Journal, 2013.

[63] Andreas Plößl et al. Wafer direct bonding: tailoring adhesion between brittle materials. *Materials Science and Engineering*, R(25):1–88, 1999.

[64] Ivy Wei Qin. Wire bonding tutorial, May 2014.

[65] G. Wiedemann R. Franz. Über die wärme-leitungsfähigkeit der metalle. *Annalen Annalen der Physik*, 165:497–531, 1853.

[66] A. Radadia et al. The fabrication of all-silicon micro gas chromatography columns using gold diffusion eutectic bonding. *J. Micromech. Microeng. 20*, 2010.

[67] Gianluca Aglieri Rinella. GTK working group meeting. October 2011.

[68] P. Rodriguez Perez. Micro-channel evaporative CO_2 cooling for the LHCb VELO Upgrade. In *Technology and Instrumentation in Particle Phyiscs*, 2014.

[69] Giulia Romagnoli. Electro-mechanical integration of a cooling device for particle detectors. Master's thesis, Università degli Studi di Genova, 2011.

[70] S. Selberherr. *Analysis and Simulation of Semiconductor Devices*. Springer-Verlag, 1984.

[71] Koji Shiomi. $K_L^0 \to \pi^0 \nu \bar{\nu}$ at KOTO. In *8th International Workshop on the CKM Unitarity Triangle (CKM2014) Vienna, Austria, September 8-12, 2014*, 2014.

[72] Swagelok. *Industrial Pressure Transducers*, April 2011.

[73] Swagelok. *Gaugeable Tube Fittings and Adapter Fittings*, March 2014.

[74] Cecilia Tarantino. Rare Kaon Decays Beyond the Standard Model. *PoS*, KAON:057, 2008.

[75] Y. Temiz et al. Two-phase cooling of 3d chip stacks. *Proceedings of the EPFL-CMI MicroNanoFabrication Annual Review Meeting*, May 2010.

[76] The BaBar Collaboration. *BaBar Technical Design Report*. 1995.

[77] The DELPHI Silicon Tracker Group. The DELPHI Silicon Tracker at LEP2. CERN-PPE/97-155, 1997.

[78] J. Thome et al. Cmosaic: 3d stacked architectures with interlayer cooling.

[79] Osamu Tonomura et al. CFD-based optimal design of manifold in plate-fin microdevices. *Chemical Engineering Journal*, 101:397–402, 2004.

[80] D.B. Tuckermann and R.F.W. Pease. *High Performance Heat Sinking for VLSI*, volume 2. IEEE Electron Device Letters, 1981.

[81] M. Turala. Silicon tracking detectors — historical overview. *Nuclear Instruments and Methods in Physics Research*, A(541):1–14, 2005.

[82] K. T. Turner. Mechanics of direct wafer bonding. In *Proceedings of the Royal Society*, volume A, pages 171–188, November 2006.

[83] B. Verlaat et al. CO_2 Cooling Developments for HEP Detectors. In *Proceedings of Science*. VERTEX 2009, Veluwe, the Nederlands, September 2009.

[84] Vishay. *Platinium SMD Flat Chip Temperature Sensor*, May 2014.

[85] Ralph L. Webb. Effect of Manifold Design on Flow Distribution in Parallel Micro-Channels. volume 2, Maui, Hawaii, USA, July 2003. ASME 2003 International Electronic Packaging Technical Conference and Exhibition.

Appendix

Appendix A

Appendix A shows the hydraulic scheme of the micro channel test stand, see figure 6.2. The figure also shows the where temperature and pressure probes and the mass flow meter are located in the circuit. Pumps, vacuum pumps, filters and valves are also shown.

Figure 6.3 shows the wiring scheme between the National Instruments readout cards and the Pt100 temperature probes on the dummy electronics. Also the pin assignment of the vacuum feedthroughs is documented.

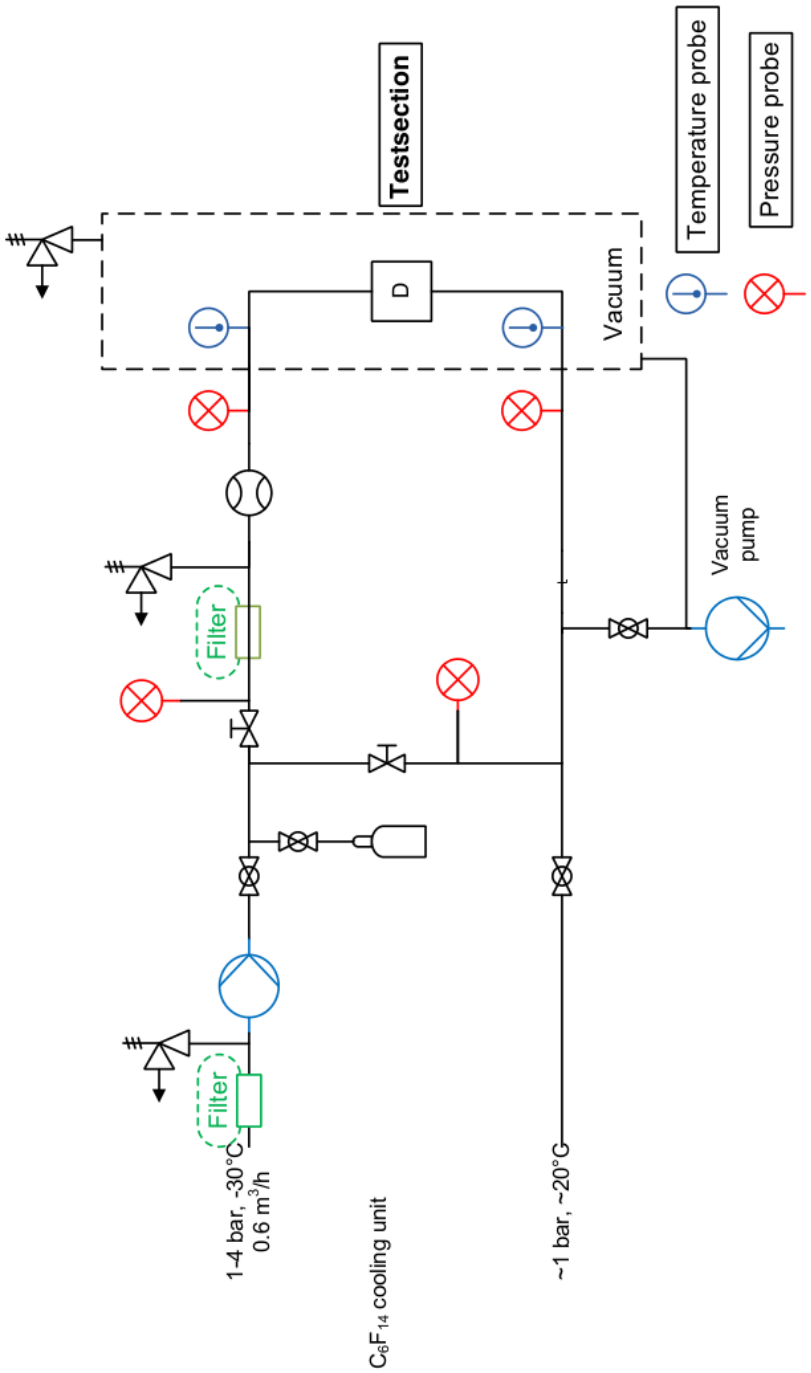


Figure 6.2: Hydraulic scheme of the test stand and the vacuum vessel piping.

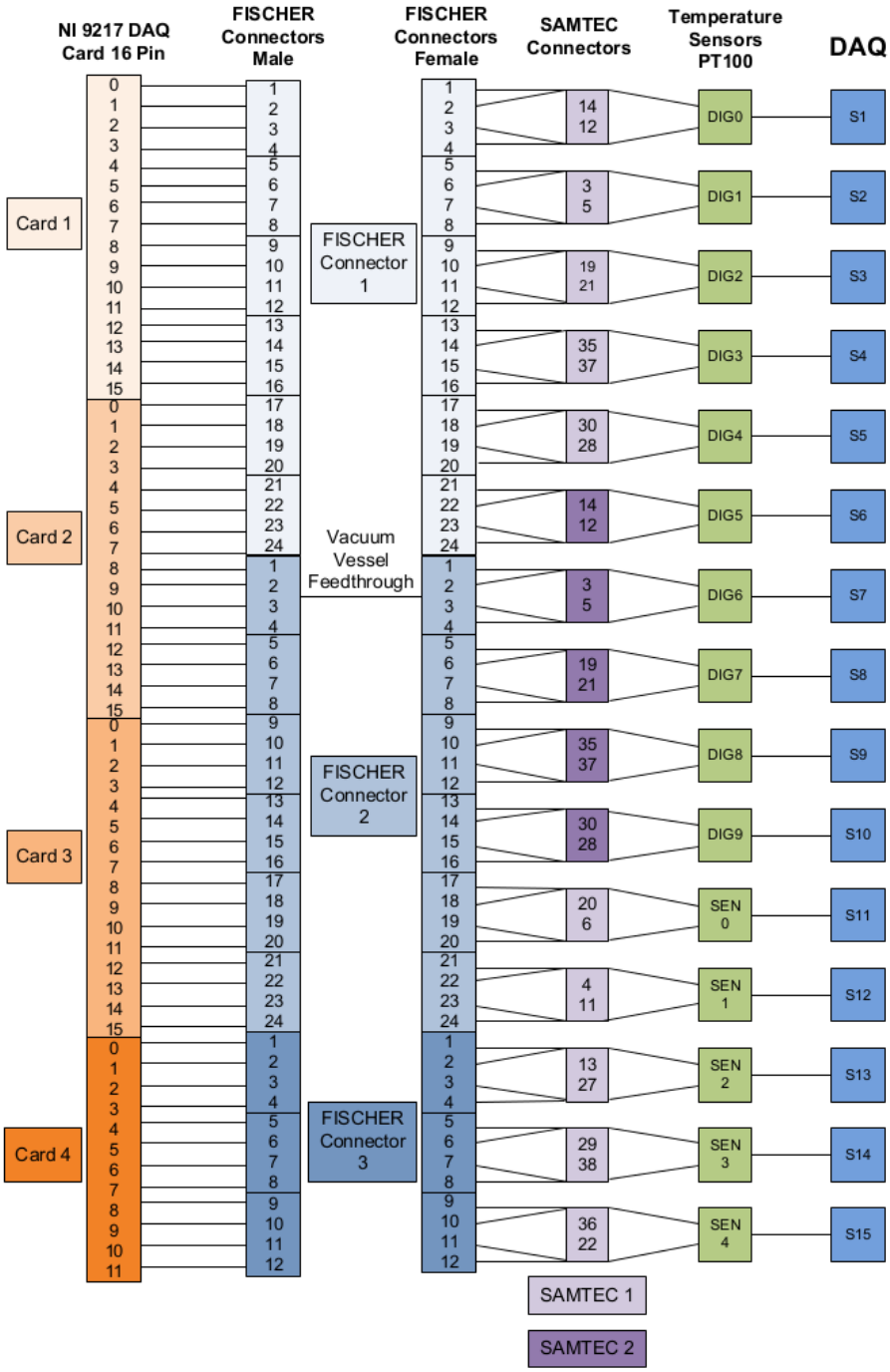


Figure 6.3: Wiring scheme for the electronics mock-up.

Appendix B

Research Project

The GigaTracKer (GTK) is a core part of the NA62 experiment and it will be installed on the SPS accelerator at CERN, Geneva. The development of a cooling system and the thermal anchoring of the GTK detector will be the major topics of this work. The detector cooling design for the three GTK stations is driven by the following requirements:

1. low detector mass with a material budget smaller than $0.5\%X_0$, which leaves the material equivalent of 150 µm of silicon to be used for cooling
2. highest temperature on the sensor should not exceed 5 °C
3. temperature uniformity of the pixel sensor should be ±3 °C
4. uniformity of the temperature across the sensor area
5. dissipated power is between 30 W and 48 W
6. system will operate in vacuum
7. pixel sensor dimensions are 27 mm x 60 mm, sensor assembly (sensor plus bump bonded readout chips) dimensions are 40 mm x 60 mm
8. 10 mm outside the sensitive area (pixel sensor surface) no material budget constraints

A cooling system with very good performance is needed to avoid thermal run-away and potential destruction of the detector module. Furthermore, it will reduce the radiation damage of the sensor and consequently increase the module life time. In this respect, although the upper limit of the operation temperature has been set to 5 °C, a lower operating temperature is highly desirable.

The proposed solution is the development of a micro channel heat sink. The micro channels are etched in the surface of a standard silicon wafer. Another wafer will be bonded with the etched wafer to form the channels. In the channels a cooling fluid will circulate and transport the heat away from the device. The detector module (Silicon pixel detector plus bump bonded readout chips) will be placed and thermally connected to the surface of the heat sink.

The material budget and the operation in vacuum are the main integration challenges of the project. The material budget constraints only concern the active beam area: therefore the mechanics and cooling integration can profit from the fact that no material budget restrictions exist for the area 10 mm outside the beam. From a cooling performance point of view, the anticipated $2\,W/cm^2$ power dissipation by the active electronics is not a difficult task to meet. The cooling and mechanics support structure must introduce a minimum amount of material into the beam area while insuring mechanical stability of the module and allowing access to high speed electrical connections.

Two recent fields of development will assist in solving the issues in engineering this cooling device. On the one hand, micro channel cooling devices have started to be actively studied for future applications for high power computing chips or 3D architectures [78],[75]; however, for these applications, where the power densities are extreme, the total radiation length of the device is an irrelevant parameter. On the other hand, thin and light micro-fluidic devices in silicon are in development for bio-chemical applications [66], but the typical values of the flow rate and pressure are much lower. In addition, the presence of a low temperature fluid and of a high radiation level is unique to the application in a HEP detector [59].

The outstanding cooling performance and its low mass are the key features making micro channels a very attractive technology for physics detectors. Research on micro channels is needed to adapt this technology to various applications.

The engineering and scientific part of the thesis work consists of

1. the conceptual and engineering design of a cooling system comprising a vacuum vessel housing the detector in the beam
2. the hydraulic and thermal layout of the micro channel heat sink and its manifold system, using analytical methods and numerical simulations (ANSYS, CFX)
3. the follow up of the prototype production of the micro channel heat sink at the clean room of the EPFL in Lausanne
4. the designs for the interfaces, distribution systems and for instrumentation

5. the building of a test setup to measure the hydraulic and thermal performance of the micro channel heat sink under conditions close to the ones in the real experiment (heat load, vacuum...)
6. the participation in the design and production of a heater mock-up that resembles the final sensor assembly as good as possible
7. the development of the integration process of a sensor assembly, a micro channel heat sink, a carrier board and a vacuum flange
8. the participation in the construction, commissioning and initial test of the system, that will be installed in the underground hall of the NA62 experiment

The work was carried out in the Cooling Group of the PH/DT Group at CERN, the GTK working group at CERN and in close collaboration with CP3 in Louvain-la-Neuve, Belgium, and the EPFL in Lausanne, Switzerland. The results shown in this thesis promise a successful implementation of the micro channel cooling techniques in other HEP experiments, e.g. the silicon tracking detectors of the LHC experiments CMS and ATLAS.