"Evaluation of monolithic pixel detector readout in silicon-on-insulator technology"

Soung Yee, Lawrence

ABSTRACT

Silicon particle detectors are found at the forefront of scientific imaging applications. From medical imaging machines that scan the human body to space telescopes observing phenomena lightyears away, silicon detectors are used in the most demanding of situations. High Energy Physics experiments, such as the ones running at CERN, use silicon pixel detectors at their core to image subatomic particles in order to probe the fundamentals of physics. Current state of the art tracker detectors are hybrid detectors which satisfy challenging resolution, material budget and radiation hardness requirements. The term hybrid refers to the fact that the sensor and readout electronics are fabricated separately and subsequently bonded together. The TRAPPISTe detector developed at the Université catholique de Louvain is a monolithic pixel detector developed in Silicon-on-Insulator (SOI) technology. As a monolithic detector, the sensor and readout electronics are fabricated on the same wafer providing potential benefits of increased resolution and lower material budget compared to hybrid detectors. The first proof of concept TRAPPISTe devices have been built and tested. A charge sensitive amplifier has been monolithically integrated into a matrix with 150um x 150um pixels. The amplifiers are able to detect 1 MIP of induced charge and the matrix is able to track the position of a laser source. These first devices show the potential of using monolithic SOI detectors in high energy physics and other applications while at the same time highlighting the technical challenges to be dealt with ...

CITE THIS VERSION

Evaluation of Monolithic Pixel Detector Readout in Silicon-on-Insulator Technology

Lawrence Soung Yee
Université catholique de Louvain

28 May 2015

Contents

Abstract

Silicon particle detectors are found at the forefront of scientific imaging applications. From medical imaging machines that scan the human body to space telescopes observing phenomena lightyears away, silicon detectors are used in the most demanding of situations. High Energy Physics experiments, such as the ones running at CERN, use silicon pixel detectors at their core to image subatomic particles in order to probe the fundamentals of physics. Current state of the art tracker detectors are hybrid detectors which satisfy challenging resolution, material budget and radiation hardness requirements. The term hybrid refers to the fact that the sensor and readout electronics are fabricated separately and subsequently bonded together. The TRAPPISTe detector developed at the Université catholique de Louvain is a monolithic pixel detector developed in Silicon-on-Insulator (SOI) technology. As a monolithic detector, the sensor and readout electronics are fabricated on the same wafer providing potential benefits of increased resolution and lower material budget compared to hybrid detectors. The first proof of concept TRAPPISTe devices have been built and tested. A charge sensitive amplifier has been monolithically integrated into a matrix with 150μm x 150μm pixels. The amplifiers are able to detect 1 MIP of induced charge and the matrix is able to track the position of a laser source. These first devices show the potential of using monolithic SOI detectors in high energy physics and other applications while at the same time highlighting the technical challenges to be dealt with such as the backgate effect and radiation hardness.

Acknowledgements

I would like to thank my mother, father and brother for all their support throughout the years. Thank you to my supervisors Prof. Eduardo Cortina and Prof. Denis Flandre for their guidance during my PhD. And a special thank you to Elena Martin and Paula Alvarez for all the hard work and the good times together inside and outside the lab.

Foreword

Silicon particle detectors are found at the forefront of scientific imaging applications. From MRI and PET machines that scan the human body to space telescopes observing phenomena lightyears away, silicon detectors are used in the most demanding of situations. They are also found at the core of high energy particle physics research, imaging subatomic particles in particle colliders. The Large Hadron Collider (LHC) at CERN in Geneva began operations in 2009 and is expected to collect data from proton-proton collisions at energies of 7 TeV per beam by 2014 [1]. Future proposed colliders such as the International Linear Collider (ILC) and Compact Linear Collider (CLIC) are being designed to provide collisions in the TeV range [2] [3]. These advanced machines are probing the fundamentals of physics by colliding particles at high energies and observing the results of the impact.

In order to observe the particle collisions, the impact points are surrounded by large particle detectors. Experiments such as CMS and ATLAS at the LHC surround the point of impact and record all the resulting particles. Large detector systems are composed of several detector subsystems designed to identify and reconstruct the path of the particles produced during the collision. The subsystem closest to the particle

beam is often referred to as the tracker, as it provides high spatial and timing resolution to allow for the positional tracking of particles.

These detectors are designed to detect particles such as muons, electrons, photons and other collision and decay products. Anywhere from 10-100 particles may emerge from a collision, some of which may only live for a picosecond before decaying. These scientific requirements lead to some challenging technical specifications in terms of resolution, radiation hardness and material budget.

- Resolution: Particle tracks should be measured as accurately as possible in time and space and as close as possible to the interaction point. For a short lived particle with a lifetime of 1 picosecond, this requires an accuracy of less than $30\mu ms$ [4]. Also, detectors within a small area are required to accurately capture all passing particles.
- Material Budget: In order to minimize the scattering of particles as they pass through the detector, it is desirable to minimize the thickness of the detectors and to reduce the amount of other material in the particle's path.
- Radiation hardness: Being positioned so close to the beam interaction point, the sensors in the tracker are exposed to high levels of radiation. For example, the innermost layer of the CMS tracker is expected to be experience a fluence of $2\times10^{14}n_{eq}/cm^2yr$ and all components are specified to be operational up to $6 \times 10^{14}n_{eq}/cm^2$ [5].

The current state of the art in tracker detectors which satisfy these requirements are silicon particle detectors. Closest to the impact point are hybrid pixel detectors. The term hybrid refers to the fact that the sensor and readout electronics are fabricated separately and subsequently bonded together. For pixel matrices, this requires the use of bump bonding techniques. Solder balls or bumps are placed on bonding pads on the sensor matrix and then aligned with bonding sites on the electronics matrix. The solder bumps are then melted to complete the bonding.

Hybrid detectors are currently performing admirably but do have some limitations for future particle physics detectors. The bump bonding pro-

cedure is a complicated and expensive one. As resolution requirements increase, the pixel size requirements decrease making it increasingly difficult to design, align and bond the two separate parts. Hybrid detectors also require two substrates which puts a limit on the material budget of the detector.

One possible solution for future detector development is to build a monolithic detector. Research into future monolithic silicon detectors is currently on-going. A monolithic detector incorporates the sensor and readout electronics in one substrate. This would eliminate the need for bump bonding, allowing the design of smaller pixels and reducing the overall thickness of the detector.

This thesis describes the first attempts to build a monolithic silicon particle detector named TRAPPISTe (Tracking Particles for Particle Physics Instrumentation in Silicon-on-Insulator Technology) at the Université catholique de Louvain. TRAPPISTe is a research and development project with the aim of studying the feasibility of developing monolithic radiation detectors in silicon-on-insulator (SOI) technology. The SOI wafer provides the possibility to integrate a sensor in a bottom handle layer with integrated electronics in a top active layer. The two layers are insulated from each other by a middle buried oxide layer resulting in sensor and readout circuitry constructed in the same silicon wafer.

The first chip in the TRAPPISTe project, TRAPPISTe-1, was developed at UCL's WINFAB facility [6]. Using the expertise in SOI technology at UCL's ICTEAM department, the first test structures were developed in a $2\mu m$ FD-SOI CMOS process. A pixel matrix was presented at the 2010 Vienna Conference on Instrumentation [7] and a charge amplifier study was presented at the 2011 IEEE International SOI Conference [8]. The second chip in the series, TRAPPISTe-2, was developed by OKI Semiconductor (now Lapis Semiconductor) in Japan in a $0.2\mu m$ FD-SOI CMOS process. As part of the SOIPIX collaboration, a pixel matrix and several test structures were produced and tested. TRAPPISTe-2 has been presented at the PIXEL 2012 [9] and TWEPP 2012 [10] conferences. These test devices are the subject of this thesis which is structured as follows:

- Chapter 1 introduces silicon detectors for particle detection. Current detector systems are reviewed and the concept of monolithic pixel detectors is introduced. SOI technology and its application in the design of a monolithic pixel detector is explained.
- Chapter 2 describes the creation of a charge sensitive amplifier for silicon detectors. A design methodology based on the g_m/I_D transistor characteristic is developed and its application to TRAPPISTe technologies demonstrated.
- Chapter 3 describes the TRAPPISTe test structures that have been fabricated. Stand alone amplifier structures with no detector attached have been produced for electrical characterization and pixel matrices with integrated readout have been fabricated for testing with a laser source.
- Chapter 4 describes the electrical measurements performed on stand alone TRAPPISTe-2 amplifier test structures. Electrical characterization and charge injection tests with input test capacitors have been made.
- Chapter 5 describes the laser measurements performed on a TRAPPISTe-2 pixel matrix. The pixel matrix includes integrated readout amplifiers and their response to charge injection with a laser source is shown.
- Chapter 6 concludes the thesis. An evaluation of the test structures is made and considerations for future TRAPPISTe devices are outlined.

CHAPTER 1

Introduction

1.1 Semiconductor Detectors

The use of semiconductors as radiation detectors can be traced back to the 1960's when germanium and silicon detectors were first used for nuclear spectroscopy. These first detectors were optimized for energy resolution and high count rate. They consisted of a single sensor, often cooled in liquid nitrogen, attached to large stand alone electronics boxes. In the 1980's, advances in microelectronics process techniques revolutionized silicon detector technology. Adapting the precise micron-scale patterning used to process microelectronic circuits, it was possible to produce arrays of sensors only a few microns wide very close together. This development permitted the design of position sensitive detectors. These segmented detectors required the development of high density front end electronics optimized for low noise, low power and minimum material use. For example, the CMS microstrip detector subsystem now contains about 6000 modules for a total of $\approx 5 \times 10^6$ channels.

One of the biggest motivators for the adoption of silicon in detector design is its widespread use in the electronics industry. Its popularity has lowered the price of the raw material and the advanced processing techniques used to make electronics can also be applied to the development of detectors. Another advantage is that since both the detector and electronics are made of silicon, integration of the two parts is easier.

1.1.1 Silicon Characteristics

Silicon as a detector medium is currently the standard for tracking detectors as it possesses many desirable qualities. As a semiconductor, silicon has a bandgap or energy range in which no electron states can exist. This is in contrast to conductors where the valence and conduction bands overlap. Insulators also possess a band gap which is much larger than those of semiconductors. As a result, much more energy is required to promote an electron to the conduction band in an insulator compared to a semiconductor. In conductors, electrons move freely into the conduction band. Figure 1.1 shows a representative diagram of the valence and conduction bands in conductors, semiconductors and insulators. The Fermi Level shown is the energy level at which the electron state occupation probability is one half at a given temperature.

A plot of the density of states in silicon reveals that between the valence band and conduction band, an energy gap of 1.12eV exists at a temperature of 300K. While 1.12eV is the minimum amount of energy required to raise an electron into the conduction band, an average of 3.6eV is required as some of the energy is lost in phonon and lattice excitations. Compared to the 30eV required for gas detectors, silicon provides a larger number of charge carriers being produced per unit energy as well as a better energy resolution.

Silicon also has a high density (2.33 g/cm^3) resulting in a large energy loss per distance traveled of an incident particle (3.8 MeV/cm for a minimum ionizing particle), which means thin detectors can be built which will produce measurable signals. The high mobility of electrons

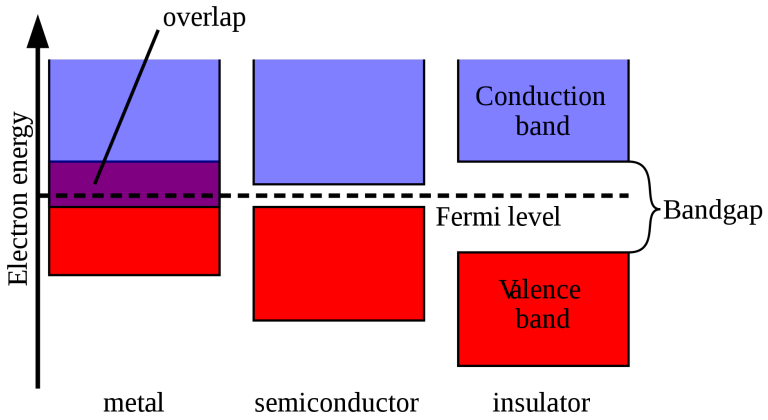

Figure 1.1: Simplified depiction of the band diagrams in conductors, semiconductors and insulators. [11]

Table 1.1: Bulk Silicon Material Properties

Density	2.33 g/cm^3
Band Gap at 300K	1.12 eV
Mean Energy for e-h pair creation	3.6 eV
Electron mobility at 300K	1450 cm^2/Vs
Hole mobility at 300K	450 cm^2/Vs

($\mu_n = 1450 cm^2/Vs$) and holes ($\mu_p = 450 cm^2/Vs$) allows for charge collection on the order of nanoseconds and its mechanical rigidity enables the construction of self-supporting structures. The material properties of silicon are listed in Table 1.1 and a more detailed description of semiconductor properties can be found in the text by Lutz [12].

An important property of semiconductors is the ability to tune their electrical characteristics by doping. An intrinsic semiconductor at thermal equilibrium has an equal concentration of electrons (n) and holes (p) so that

$$n = p = n_i \tag{1.1}$$

where n_i is called the intrinsic carrier density. For silicon at a temperature of 300K the intrinsic carrier density is $1.45 \times 10^{10} cm^{-3}$.

By introducing impurities into a pure or intrinsic semiconductor, the carrier concentrations within the semiconductor can be changed. In a doped or extrinsic semiconductor, the electron (n_0) and hole (p_0) concentrations follow [12]

$$n_0 = n_i e^{\frac{E_F - Ei}{kT}} \tag{1.2}$$

$$p_0 = n_i e^{\frac{E_i - EF}{kT}} \tag{1.3}$$

where E_i is the intrinsic silicon Fermi level and E_F is the Fermi level in the doped semiconductor. The carrier concentrations also obey the mass action law [12]

$$n_0 \cdot p_0 = n_i^2 \tag{1.4}$$

Two types of doped semiconductor can be produced: n-type or p-type. N-type semiconductors have higher electron concentrations than hole concentrations and are produced by doping an intrinsic semiconductor with donor atoms, typically phosphorus or arsenic. P-type semiconductors are doped with acceptor atoms such as boron and have higher hole concentrations than electron concentrations. Increasing the doping concentration increases the number of carriers available for conduction thus increasing the conductivity of the material.

1.1.2 The P-N Junction

The most basic semiconductor detector is essentially a diode. A p-n junction is created in a semiconductor by p-doping an n-type substrate or vice versa. At the junction between the n and p type layers, the majority carriers from one side will diffuse to the other due to the difference in carrier concentration. The majority carriers will recombine, leaving behind a depletion zone in which acceptor and donor ions are present

without their free charge carriers. The depletion region, also known as the space charge region, is electrically charged resulting in an electrical field which counteracts the diffusion of carriers as shown in Figure 1.2. The maximum electric field E_{max} is given by

$$E_{max} = \sqrt{\frac{2q}{\epsilon}\frac{N_A N_D}{N_A + N_D}V_{bi}} \tag{1.5}$$

where ϵ is the permittivity.

This results in a built-in voltage V_{bi} which can be calculated as

$$V_{bi} = \frac{kT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right) \tag{1.6}$$

where k is the Boltzmann constant, T is the absolute temperature, N_D is the donor concentration and N_A is the acceptor concentration.

If an external voltage is applied in the same direction as the built-in voltage, more free carriers will be removed and the depletion zone will be increased. The junction is now reverse biased and the width of the space charge region (d) will be given by

$$d = \sqrt{\frac{2\epsilon}{q}\left(\frac{N_A N_D}{N_A + N_D}\right)(V_{bi} + V)} \tag{1.7}$$

where V is the applied external voltage, so that the depletion width increases with more reverse bias voltage.

The full depletion voltage is the voltage required to create a depletion region that covers the entire thickness of the detector. As many detectors are operated in full depletion, the full depletion voltage is an important parameter to consider during sensor design. From Equation 1.7, one can see that the depletion width depends on the doping of the material. This property is often expressed in terms of resistivity ρ which is equal to

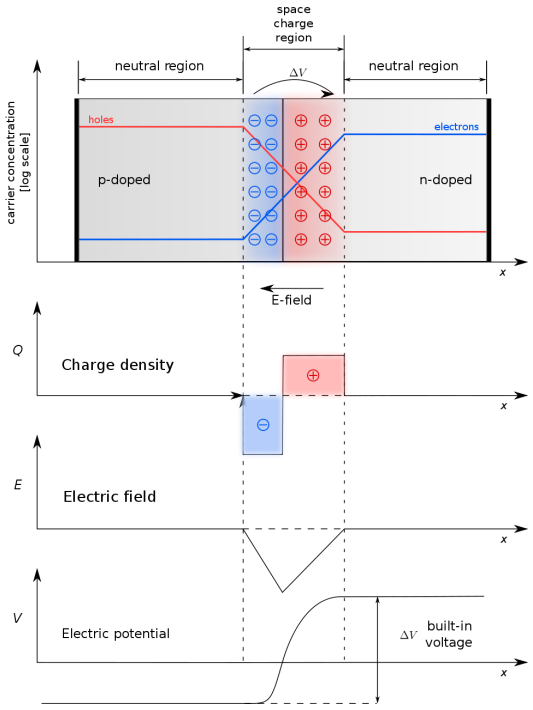

Figure 1.2: PN Junction and Depletion Zone [13]

$$\rho = \frac{1}{eN\mu} \tag{1.8}$$

where e is the electron charge, N is the dopant carrier concentration and μ is the mobility of the majority carrier. Resistivity is typically expressed in terms of Ωcm. For a given bias voltage, a substrate with higher resistivity is easier to deplete than a lower resistivity substrate. For silicon radiation detectors, resistivity values from 5k to 20k Ωcm are common [14].

Depletion also plays an important role in the amount of dark current or leakage current present in the p-n junction. Even in the absence of external radiation, a current is present in the reversed biased diode. The leakage current is a result of several mechanisms but tends to be

dominated by thermal generation at generation-recombination centers in the depletion area [4]:

$$J_{vol} \approx -e\frac{n_i}{\tau_g}d \tag{1.9}$$

where J_{vol} is the volume generation current per unit area, τ_g is the carrier generation lifetime and d is the depletion width. The leakage current is an important factor to consider as it contributes to the noise of a detector system as shown in Chapter 2.

While fully depleting and even overdepleting the detector may be desirable, overdepleting the substrate too much can lead to electrical breakdown. Electrical breakdown can occur due to two mechanisms: Zener breakdown or avalanche breakdown. In Zener breakdown, the electric field is strong enough to directly liberate covalently bound electrons in the material, promoting them from the valence band to the conduction band. In avalanche breakdown, free charge carriers gain enough energy in the high electric field to break covalent bonds in the material when they collide. This results in the creation of two more carriers, an electron and a hole, that will also accelerate in the field and in turn liberate more covalently bound carriers causing a multiplication or avalanche effect. Both breakdown mechanisms result in a high reverse current which can permanently damage the semiconductor material.

1.2 Radiation Interactions with Matter

The detection of incident radiation by a semiconductor relies on the fact that radiation incident upon semiconductor material causes the creation of electron-hole pairs. These pairs induce charge within the semiconductor that can be measured as an electrical signal. Electron-hole pairs are created by different mechanisms which depend on the type on incident particle and the speed of the incoming particle. A detailed description of the interaction of radiation on matter can be found in the Review of Particle Physics by the Particle Data Group [14].

1.2.1 Charged Particles

For incident charged particles such as heavy ions, protons and muons, interactions within target matter mostly occur between the incident particle and electrons in the semiconductor lattice. Interactions between incident particles and atomic nuclei do occur but they are relatively rare and are of less interest to radiation detectors. As the charged particle passes through the material, it exerts a coulomb force on nearby electrons which may excite the electron to a higher energy state or remove the electron from the atom if enough energy is transfered. Removal of an electron from the atom is called ionization and results in an electron-ion pair being created.

As the particle continues on its path, it will continuously impart its energy to neighboring electrons and slow down, eventually leaving the material or stopping in it if it loses all of its velocity. For heavy charged particles, the path taken by a charged particle is generally straight as it is not greatly deflected by any one interaction and interactions occur simultaneously in all directions.

1.2.1.1 Ionization Loss

For charged heavy particles, the mean rate of energy loss due to ionization can be described by the Bethe equation [14]

$$-\frac{dE}{dx} = Kz^2\frac{Z}{A}\frac{1}{\beta^2}\left[\frac{1}{2}\ln\frac{2m_ec^2\beta^2\gamma^2T_{max}}{I^2} - \beta^2 - \frac{\delta}{2}\right] \tag{1.10}$$

where T_{max} is the maximum kinetic energy which can be imparted to a free electron in a single collision given by

$$T_{max} = \frac{2m_ec^2\beta^2\gamma^2}{1 + 2\gamma\frac{m_e}{M} + (\frac{m_e}{M})^2} \tag{1.11}$$

Table 1.2 details the variables used in the Equations 1.10 and 1.11 for an example calculation of a incident muon on silicon.

Variable	Definition	Value	Units
$\frac{dE}{dx}$	Energy loss	-	$MeVg^{-1}cm^2$
c	Speed of light in vacuum	2.998×10^8	m/s
$m_e c^2$	Electron mass X c^2	0.510	MeV
r_e	Classical electron radius	2.818	fm
N_A	Avagadro's number	6.022×10^{23}	mol^{-1}
K	$4\pi N_A r_e^2 m_e c^2$	0.307	$MeVg^{-1}cm^2$
z	Charge of incident particle	-1	-
Z	Atomic number of target material	14	-
A	Atomic mass of target material	28.0855	-
β	Relative speed of the incident particle v/c	-	-
v	Speed of the incident particle	-	ms^{-1}
γ	Relativistic dilation factor $1/\sqrt{1-\beta^2}$	-	-
I	Mean excitation energy	173	eV
δ	Density effect correction (energy dependent)	-	$MeVg^{-1}cm^2$
M	Incident particle mass	105.65839	MeV/c^2

Table 1.2: Summary of variables for Equations 1.10 and 1.11. These values show an example calculation for an incident muon on silicon. [14]

From the Bethe equation, the energy loss rate depends very little on the incident particle mass as shown in the T_{max} definition. Also, for most target materials, the Z/A ratio is nearly constant so the energy loss rate

is almost independent of the target material. The most important factors determining the energy loss rate are the particle charge z and speed β expressed as a fraction of the speed of light.

A plot of the Bethe formula reveals that as the energy of an incident charged particle increases, the energy loss per path length decreases, eventually reaching a minimum plateau. Figure 1.3 shows the plot the mean ionization energy loss of a muon in silicon material (also shown is the radiative loss, described in the following Section 1.2.1.2). One can see that in the Bethe plot, the function reaches a broad minimum point. Particles exhibiting this minimum energy loss are referred to as minimum ionizing particles (MIPs). In the particular case of silicon, a MIP produces about 80 electrons per micrometer of material.

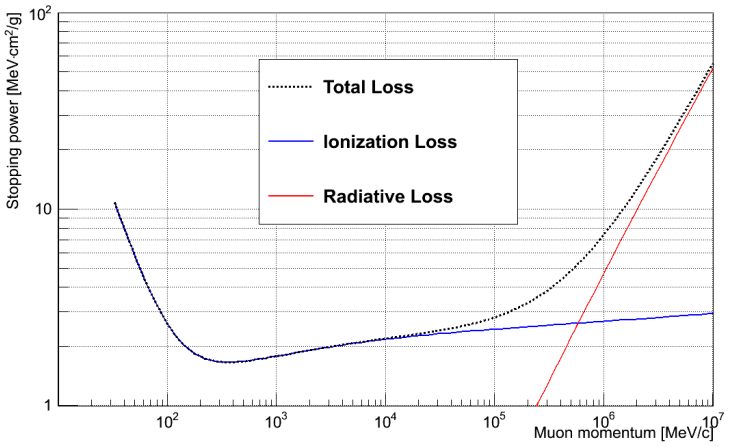

Figure 1.3: Stopping power for positive muons in silicon. At lower energy ranges, energy loss is dominated by ionization losses. Data taken from [15].

1.2.1.2 Radiative Loss

Radiative loss is the main energy loss mechanism for electrons and at high enough particle energies, radiative losses also become more important

for heavier charged particles. The point at which ionization losses and radiative losses are equal is often referred to as the critical energy. For electrons and muons in silicon, the critical energy is low enough to be of concern in current particle detectors. For particles heavier than a muon, the critical energies are much higher and radiative losses are of less concern. Figure 1.4 shows that for the specific case of muons in silicon, radiative losses start to dominate the total amount of energy loss after an incident momentum of around $5.8 \times 10^5 MeV/c$.

The main contributions to radiative energy losses are

- **Bremsstrahlung**: When light charged particles such as electrons and muons enter matter, they may be deflected by charged atomic nuclei. This causes the incident particle to decelerate and lose kinetic energy. A photon is produced to conserve energy. The energy imparted to the photon is equal to the kinetic energy lost by the incident particle so that larger energy losses result in higher frequency photons.
- **Pair production**: Pair production can occur when an incident particle interacts with a nucleus and decays into another particle and its antiparticle. For example, a photon can decay into an electron and positron provided the incident photon has an energy greater than the rest mass of the two produced particles. If the photon has energy greater than the required minimum energy, the extra energy is imparted into the two resultant particles as kinetic energy.
- **Photonuclear**: At very high energies, light particles such as electrons may interact directly with the atomic nuclei in the target material. For electrons, photonuclear effects start to dominate radiative losses for energies above 10^{21} eV [14].

A plot of the average energy loss due to radiative losses of a muon in silicon is shown in Figure 1.4. Pair production and bremsstrahlung losses are the biggest contributors in the shown energy range.

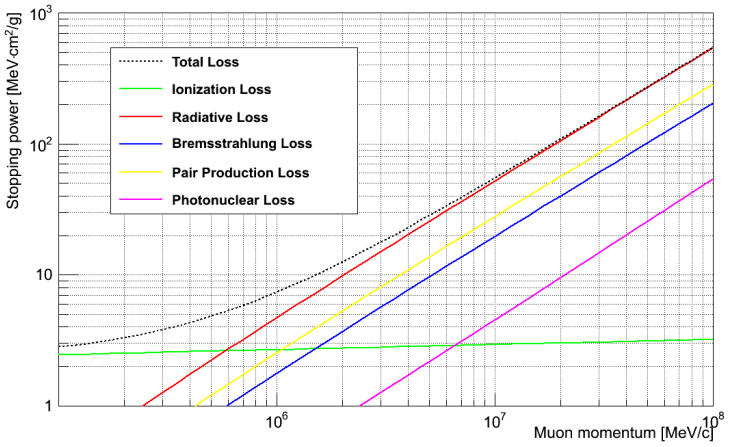

Figure 1.4: Stopping power for positive muons in silicon showing radiative losses at high energies. Data taken from [15].

1.2.1.3 Straggling

While the Bethe formula describes the mean energy loss of a particle through matter, when describing energy loss for a single particle the most probable energy loss is more useful experimentally. For a material of thickness x, the energy loss of an incident particle in the material follows a probability distribution which is highly skewed. The most probable energy loss is found to be lower that the mean value found from the Bethe formula, as rare high energy transfer collisions lead to a long tail in the distribution function. A plot of the probability function for a 500 MeV pion in silicon is shown in Figure 1.5. One can see that the most probable loss denoted Δ_p/x is below the mean energy loss and that as the material thickness increases, the width W of the distribution also increases.

The most probably energy loss can be calculated by

$$\Delta_p = \xi \left[ln\frac{2mc^2\beta^2\gamma^2}{I} + ln\frac{\xi}{I} + j - \beta^2 - \delta \right] \tag{1.12}$$

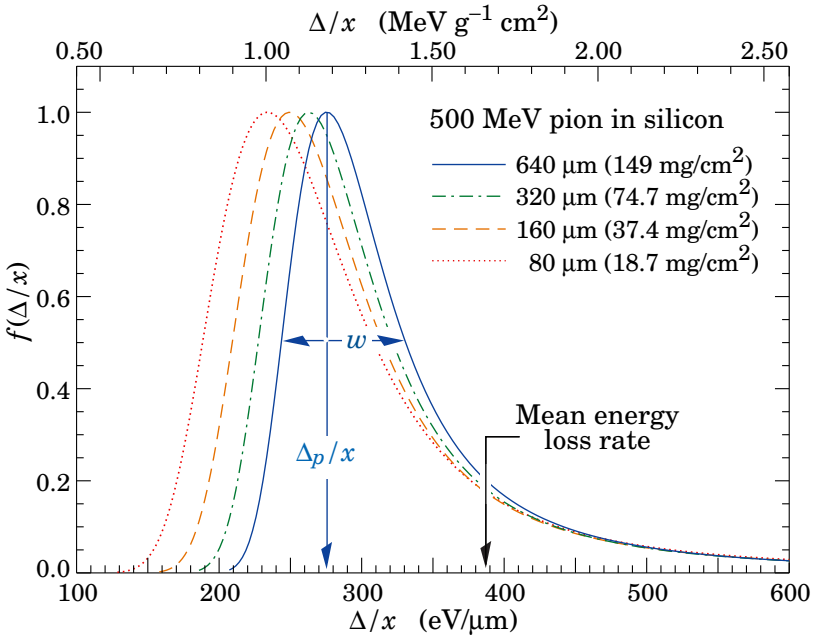

Figure 1.5: Straggling function for a 500 MeV pion in silicon at different thicknesses normalized to the most probable value [14].

where $\xi = (K/2)(Z/A)(x/\beta^2)$ MeV, x is the detector thickness in $g{\cdot}cm^{-2}$ and $j = 0.200$ [14]. The most probable energy loss is a more useful measure of the amount of energy loss in a thin absorber.

1.2.2 Multiple Scattering

As a charged particle goes through material, it is deflected from its initial path by several small interactions. The majority of these interactions are a result of Coulomb scattering with nuclei so the effect is known as multiple Coulomb scattering. The resulting scattering angle can be described by a Gaussian distribution with a standard deviation described by

$$\Theta_0 = \frac{13.6MeV}{\beta cp} z\sqrt{x/X_0}\,[1 + 0.038\ln(x/X_0)] \tag{1.13}$$

where β, p and z are the velocity as a fraction of the speed of light, momentum and charge number of the incident particle. The term x/X_0 describes the thickness of the material x in terms of radiation lengths X_0. The radiation length is defined as both the mean distance over which a energetic electron loses all but $1/e$ of its energy by bremsstrahlung and 7/9 of the mean free path for pair production by an energetic photon [14]. The radiation length is usually measured in $g \cdot cm^{-2}$ and for silicon its value is 21.82 $g \cdot cm^{-2}$.

For particle tracking detectors, multiple scattering is an important consideration. Scattering adds uncertainty to the reconstruction of the particle's flight path and therefore reduces the precision of the spatial measurement. From the scattering equation 1.13, one can see that the thicker the material is, the larger the spread in scattering angles is. It is therefore desirable to decrease the amount of material a particle passes through in the tracker.

1.2.3 Photons

Photons interact with matter differently than charged particles. The processes of main interest to semiconductor radiation detectors are the photo-electric effect, coherent scattering, Compton scattering and pair production.

- The photo-electric effect occurs when an incident photon interacts with an absorber atom and completely disappears. An energetic photo-electron is released from one of the atom's bound shells. The photo-electron released has an energy equivalent to the energy of the incident photon minus the binding energy of the photo-electron to its shell. Left behind is the ionized atom with a vacancy. This vacancy can be filled by a free electron or rearrangement of the atoms electrons which may generate X-ray photons.

- Coherent scattering occurs when an incident photon is completely absorbed by a atomic electron and another photon is re-emitted by the excited electron. The newly released photon has the same energy as the original photon so no energy is absorbed by the atom. The direction of the outside new photon is arbitrary, resulting in scattering.
- Compton scattering occurs when an incident photon scatters off an electron in the target material. The photon will impart a portion of its energy to the electron, which will recoil with a higher energy and is often referred to as the recoil electron. Depending on the angle of incidence, the photon may impart almost none to almost all of its energy to the electron.
- For photon energies higher than 1.02 MeV, it is possible for pair production to occur. In pair production, which occurs within the Coulomb field of a nucleus, the photon disappears and is replaced with an electron-positron pair. The shared energy of the resulting pair is equal to the energy of the incident photon minus 1.02 MeV. The created positron will eventually annihilate producing two secondary photons. The probability of pair production occurring at lower energies is very low and only becomes significant at energies above around 5MeV.

Figure 1.6 shows the energy dependence of the different attenuation coefficients for photons in silicon. At low photon energies, the photoelectric effect and coherent scattering dominate while at high energies above 10 MeV, pair production dominates. In between, Compton scattering is the main process for interaction.

Semiconductors detectors can be characterized with photons by the use of laser systems. For a silicon detector of $300\mu m$ thickness, one can simulate a MIP using an infrared laser at around 1060nm. At this wavelength, the photon energy is about equal to the silicon bandgap energy of 1.1 eV. Figure 1.7 shows the absorption depth of light in silicon as a function of wavelength and shows that for infrared light the absorption depth of a photon is close to $300\mu m$. Light at lower wavelengths would be absorbed

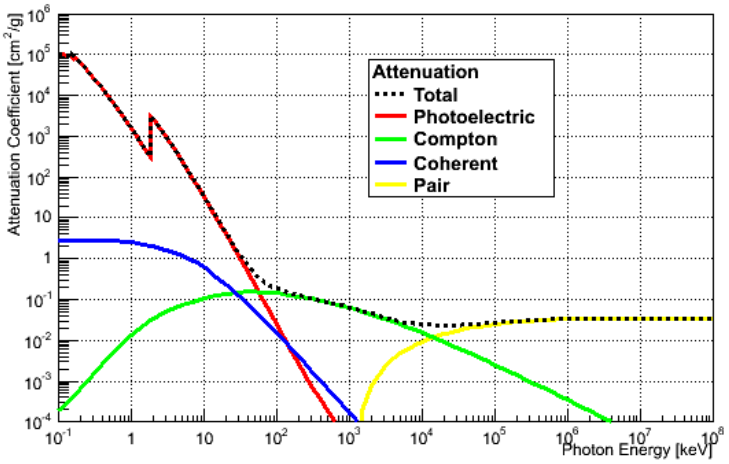

Figure 1.6: Attenuation coefficient for photons in silicon. Data taken from [16].

in the first few microns of detector and longer wavelengths would pass through the detector. The collected charge due to the light interaction is used to calibrate the detector and the intensity of the laser can be tuned to deliver a known number of photons.

1.3 Signal Formation in Semiconductors

To detect the passage of particles through a detector, one has to be able to detect the energy deposited in the material by the incident particle. For semiconductors, the electron-hole pairs created by energy deposition are detected. In silicon, electrons having more energy than 1.12 eV may cross the bandgap and go into the conduction band. However, an average of 3.6 eV of deposited energy is required to create an electron-hole pair as some energy is lost as heat and in lattice excitation.

It is important to note that ambient thermal excitation also leads to electron promotion resulting in a background signal. The number of free

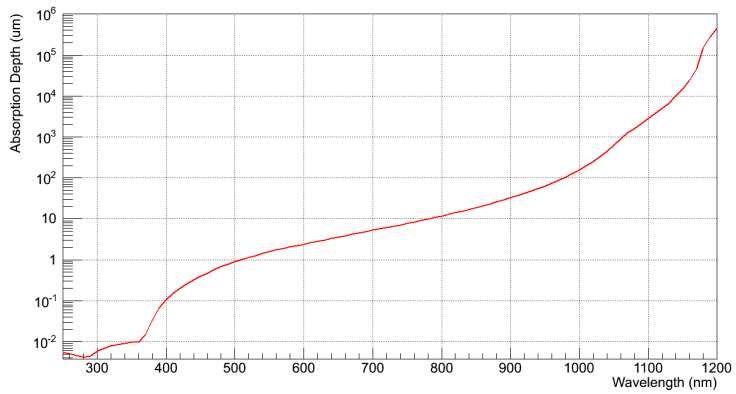

Figure 1.7: Absorption depth for photons in silicon. Infrared light at 1060nm is typically used to simulate a MIP in 300μm thick detectors. Data taken from [17].

carriers in a semiconductor is dependent on temperature (Equations 1.2 and 1.3) so that higher temperatures result in a larger number of carriers. This background limits the detector resolution and is an important design parameter to consider.

The electrons and holes created during ionization will recombine if they encounter other holes and electrons. If they are created in intrinsic unbiased silicon, the new carriers would quickly recombine with other carriers in the material and virtually no signal would be detected. The creation of the depletion zone introduces an area where few other carriers are present, reducing the probability of recombination. As a result, operating the detector at full depletion voltage is usually the optimal operating condition.

Under normal detector operation, the detector is biased resulting in an electric field in the semiconductor. The electron-hole pairs created during ionization will move in the electric field according to diffusion and drift:

- Diffusion: Carriers move randomly due to thermal motion but in the presence of a concentration gradient, the net motion is towards the area of lower concentration.

- Drift: Carriers move parallel to the electric field according to $\vec{v} = \mu\vec{E}$, where μ is mobility.

Due to different electron and hole mobilities, the carriers will drift and diffuse towards the anode and cathode of the detector at different rates. The total time taken to reach the electrodes is called the charge collection time.

Although the carriers take time to move in the detector, the signal on the electrodes is produced as soon as the charge carriers are created. The created electron-hole pairs induce charge on the electrodes as soon as they appear in the body of the detector. This is described by the Shockley-Ramo theorem [18].

$$i = q\vec{v} \cdot \vec{E}_W = q\mu\vec{E} \cdot \vec{E}_W \tag{1.14}$$

where i is the induced current, q is the electron charge, $\vec{E}$ is the electric field and $\vec{E}_W$ is a weighting field. The weighting field describes the way the charge motion couples to an electrode and is dependent on the geometry of the detector and electrodes. It is a geometrical construct and can be calculated for a given electrode by setting a given electrode to 1V and all other electrodes to 0V and calculating the resulting electric field in a vacuum as shown in Figure 1.8. The geometry calculated in Figure 1.8 is a 400 μm thick detector with a top electrode located in the middle of the detector. The weighting field was calculated using Synopsis TCAD software [19] which enables the simulation of semiconductor device physics.

Calculating the charge induced on an electrode can be done by following the created carrier carriers as they drift in the detector and applying the Schockley-Ramo theorem at each point in time. A typical plot of an induced signal is shown in Figure 1.9 generated by the Weightfield2 program [20]. This example shows the collection of one MIP in a 300μm thick fully depleted pad detector. One can see that the electrons (shown by the red line) are more quickly collected than the holes (shown by the

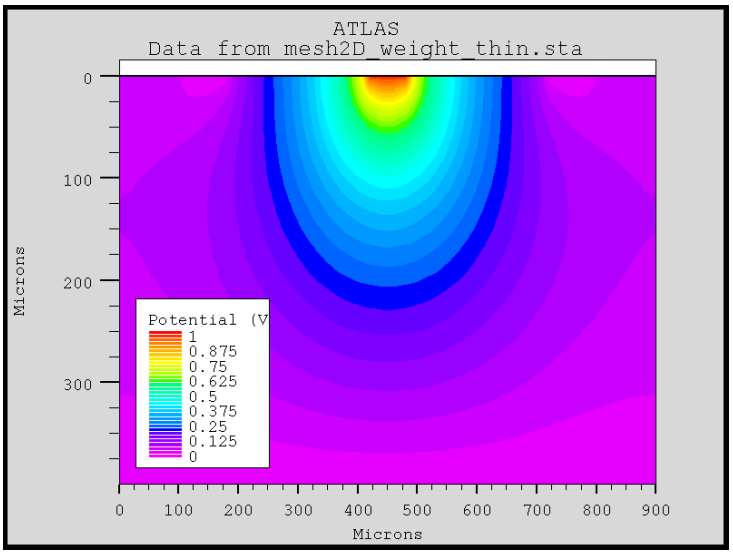

Figure 1.8: 2D weighting field for a top electrode calculated in TCAD [19]

blue line) due to their higher mobility. The signal is induced immediately and decays as the carriers arrive at the electrode.

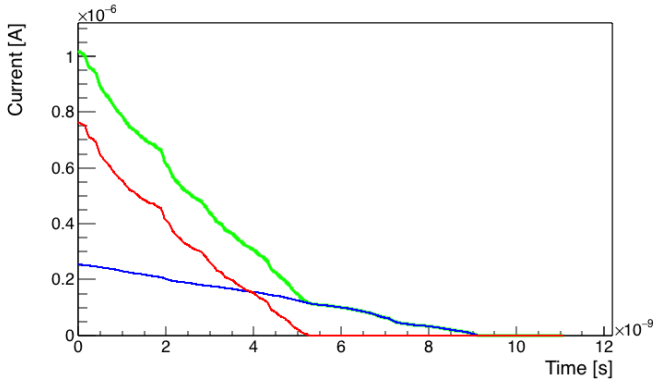

Figure 1.9: Induced signal calculated with Weighfield2 [20]. Electrons shown in red, holes in blue and total shown in green.

1.4 Radiation Damage in Silicon Detector Systems

While the interaction of radiation with semiconductors allows the use of semiconductors as detectors, these interactions also cause detrimental effects to detector systems. Tracking detectors close to the particle beam at the LHC are expected to be exposed to up to $2 \times 10^{14} n_{eq}/cm^2 yr$ [5] of radiation causing significant changes to the detector performance over its lifetime.

1.4.1 Silicon Detector Degradation

Radiation damage to the silicon detector material can be generally categorized into two types: Ionizing Energy Loss (IEL) and Non Ionizing Energy Loss (NIEL). IEL results in surface damage, causing positive charge buildup in SiO_2 and leading to interface states at the Si/SiO_2 interface. This can impact the detector capacitance [21] and increase 1/f noise, raising the total system noise level .

NIEL damage results when a Si atom is displaced from its substitution site, creating crystal defects in the silicon bulk. Depending on the type and energy of the incident particle, the resulting damage can range from single isolated defects, where interstitials and vacancies interact with each other or impurities in the silicon, to large area defect clusters [22]. These defects manifest themselves as degradation effects in detector performance:

- Deep level defects act as generation and recombination centers, which leads to an increase in the detector leakage current and consequently an increase in detector noise and power consumption.
- Defects result in a change in the effective doping concentration of the silicon material, changing the internal electric field profile and the bias voltage required for detector depletion.

- An increase in charge carrier traps reduces the effective carrier drift length and thereby reducing the charge collection efficiency of the detector.

Radiation effects change over time at room temperature, referred to as annealing. While over time leakage current and electron trapping effects anneal in a beneficial manner, hole trapping is further increased. The effective doping concentration is affected over time by a buildup of negative space charge, which can be detrimental to Float Zone type silicon detectors but can be beneficial to Czochralski and Epitaxial Silicon detectors [21].

The performance of silicon detectors after intense radiation is increasingly important as higher luminosity detectors are built. Research projects such as the RD50 collaboration at CERN study different techniques and materials to develop radiation-hard sensors [23].

1.4.2 Effects on Electronic Devices

Radiation effects on electronic circuits can be divided into two categories: Total Ionizing Dose (TID) and Single Event Effects (SEE). TID effects are characterized as longterm effects appearing over time while SEEs are instantaneous effects due to an incident particle.

TID effects build up over time as a device is exposed to ionizing radiation. This can result in the accumulation of positive charge in oxides, causing shifts in transistor threshold voltages and increased leakage currents resulting in more noise [24].

SEEs result from a single ionizing particle depositing enough energy in a sensitive semiconductor region of a device to cause a change in behavior of a device. SEEs can result in soft errors which are recoverable or hard errors which result in permanent damage. Soft errors include Single Event Upsets (SEU) such as bit flips in computer memory or transients at the output of a logic or I/O circuit. Techniques such as Error Correction and Detection (EDAC) schemes are often employed in systems susceptible to SEU events. More problematic are hard errors which results in

irreversible damage. Single Event Latch-ups (SEL) can result in a switch or bit to be stuck in one position which may require power cycling. Single Event Burnout (SEB) and Single Event Gate Rupture (SEGR) can result in permanent destruction of a device. A passing particle deposits enough energy to cause electric field breakdown or an increase in current beyond device tolerances, resulting in permanent damage. These last two effects are typically found in large power MOSFETs [25].

Radiation effects on devices and circuits are an important concern in the development of radiation detectors as the readout electronics get closer to the interaction point. In particular, monolithic detectors have their readout electronics placed directly next to the detector on the same wafer, increasing their exposure to ionizing radiation.

1.5 Types of Semiconductor Detectors

Semiconductor detectors come in various forms, which can be generally categorized into three categories: pad detectors, strip detectors and pixel detectors. Each has its own advantages and challenges that need to be considered for different applications.

Different types of semiconductor material besides silicon may be used when creating detectors. Diamond displays high radiation hardness and low drift currents but the material is very expensive and difficult to fabricate as large crystals. Germanium and high purity germanium detectors (HPGe) are commonly used in nuclear physics for spectroscopy, in particular gamma rays. In silicon and germanium of normal purity, depletion depths of a few millimeters can be realized before breakdown voltages occur. For the detection of gamma rays, depletion depths of a few centimeters are required [26]. This can be accomplished with very high purity semiconductors such as HPGe as can be seen from Equation 1.7. The main disadvantage of germanium is that due to its small bandgap of 0.7 eV, germanium detectors must be cooled down to liquid nitrogen temperatures as at higher temperatures they produce too much leakage current and thus too much noise [26].

Silicon is currently the semiconductor of choice for particle tracking experiments, benefiting from advanced processing techniques used in the microelectronics industry. Using silicon to reconstruct particle tracks was pioneered in the early 1980's with the NA11 project at CERN, when the detectors for the vertex tracker at the ALEPH experiment at the Large Electron Position Collider (LEP) were produced in silicon [27]. Since then, silicon has been extensively used for tracking detectors in experiments such as CDF and D0 at the Tevatron [28] [29] and currently the CMS and ATLAS experiments at the LHC [30] [31]. Space based detectors such as PAMELA [32] and AMS [33] also incorporated silicon detectors for tracking purposes with the AMS-02 Silicon Tracker having an sensible area of $6.2m^2$ of silicon [34]. The largest silicon detector is currently housed at CMS which holds over 200 m^2 of silicon detectors [35].

Typical modern silicon detectors, such as those employed at the CMS experiment, have thicknesses ranging from 300 μm to 500 μm [36]. They are made from high resistivity silicon ranging from 1 $k\Omega{\cdot}cm$ to 6.5 $k\Omega{\cdot}cm$ which requires depletion voltages below 300V [37].

1.5.1 Pad Detectors

The most basic type of semiconductor detector is a large diode, often called a pad detector. This type of detector may be used for counting events or in spectroscopy to determine the energy of an incident particle. A pad detector is created by introducing a p-implant in an n-substrate or vice versa (see Figure 1.10) to develop a space charge region as described in section 1.1.2. The first such detectors using semiconductor industry planar technology were developed by Kemmer in the early 1980's [38].

In principle, an unbiased diode could act as a detector although in practice difficulties arise from the small sensitive volume due to the thin space charge region. Also, an unbiased diode presents a high capacitive load to the readout electronics which results in increased noise, as will be discussed in Chapter 2.2.2. Instead, semiconductor detectors are usually

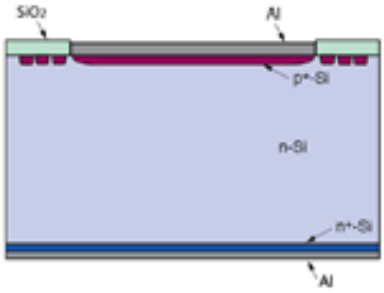

Figure 1.10: Pad detector

biased to increase their charge collection efficiency by enlarging the space charge region. Incident particles can be counted by simply observing the induced signals in the detectors. For spectroscopy, the amount of energy deposited in the detector can be obtained by measuring the amplitude of the induced signal.

1.5.2 Strip Detectors

To obtain spatial information such as required in particle tracker systems, several detectors are required such as those found on strip detectors. On a strip detector, several relatively thin and long implants are made on the detector substrate as shown in Figure 1.11. The first such detectors were developed in the early 1980's at CERN [39] and have since then become standard detectors in particle tracking systems. In modern detector systems such as CMS, the width of these strips may only be a few micrometers [40], therefore strip detectors are commonly referred to as microstrip detectors. Microstrips may be developed as p^+-strips on an n-type substrate or n^+-strips on a p-type substrate although the latter requires extra p-implants to be processed between the n-strips. The interstrip p-implants are required to prevent the build-up of electrons under the positively charged field oxide from shorting the n^+ strips [41].

The position of the incident particle can be determined by measuring which strips produced a signal. The precision of the position measure-

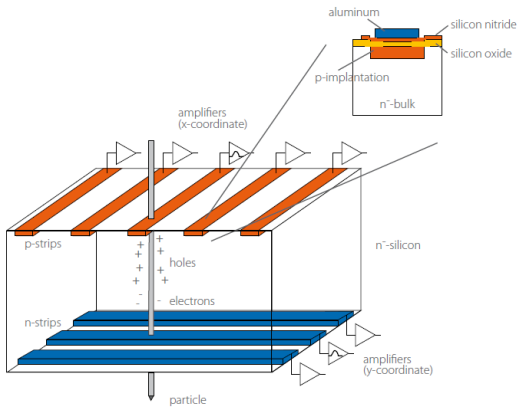

Figure 1.11: Double sided microstrip detector [42]

ment depends on the geometry of the detector, specifically the distance between the strips called the pitch (p). If only a digital yes/no signal is recorded, then the measurement precision or the root-mean-square deviation from the true position can be shown to be: $< \Delta x^2 >= p^2/12$ [12]. A more precise measurement can be made by employing an analog readout of each strip. For analog readout, the measurement precision is approximately the product of the Noise-to-Signal ratio (N/S) and the strip pitch: $\Delta x \approx (N/S)p$ [12]. If the strip pitch is fine enough so that the charge is collected over several strips, the position of the particle can be determined by interpolation of the strip signals. Typical pitch distances are a few tens to a few hundred micrometers, resulting in spatial resolutions of a few micrometers.

Double sided strip detectors allow for projective two dimensional measurements. Strips are implanted on both sides of the detector, with the top strips laid perpendicular to the bottom ones as in Figure 1.11. As a particle crosses the detector, hole and electrons are created in equal number with the electrons moving toward the n^+ implants and the holes moving toward the p implants. The strip signals from both sides of the detector are then interpolated, providing double the information for the same detector thickness. This advantage comes at the cost of more dif-

ficult processing techniques. To make a working detector, not only do both sides of the detector need to be processed and handled properly, extra p-implants need to be processed between the n^+ strips to prevent shorting due to electron build-up under the field oxide.

1.5.3 Pixel Detectors

To achieve higher two dimensional granularity, a pixel detector can be used. A pixel detector consists of a matrix of detectors, often in a grid layout. Each pixel produces its own signals, providing a large number of sensing elements in a small area which is particularly useful for recreating particle tracks. In general, two types of pixel detector technologies are used: CCD (charge coupled devices) and CMOS (complementary metal oxide semiconductor). CCD devices are ubiquitous in commercial digital cameras but have seen limited use in particle physics tracking. The first CCD trackers were developed by the ACCMOR collaboration in the 1980's [43] and the SLAC Large Detector (SLD) used CCD detectors [44]. CCD-based detectors named ISIS are also being studied for the future ILC [45]. CMOS technology is currently the more prevalent pixel technology in high energy physics trackers as it provides for faster particle tracking, up to millions of images per second, and better radiation tolerance [4].

Figure 1.12 shows how layers of pixel detectors are used to reconstruct the events of a particle collision. Point V indicates the vertex of the primary collision in a particle collider which creates several secondary particles. Point D indicates the point where one of the secondary decays. In order to accurately reconstruct the event, the pixel detectors require enough accuracy to pinpoint the origin of the passing particles. Combined with information from other detectors in the detector system, the type and position of all the particles can be identified to properly reconstruct the collision event.

Silicon pixel detector development for particle tracking was part of a validation campaign at CERN in the RD19 collaboration [46] which be-

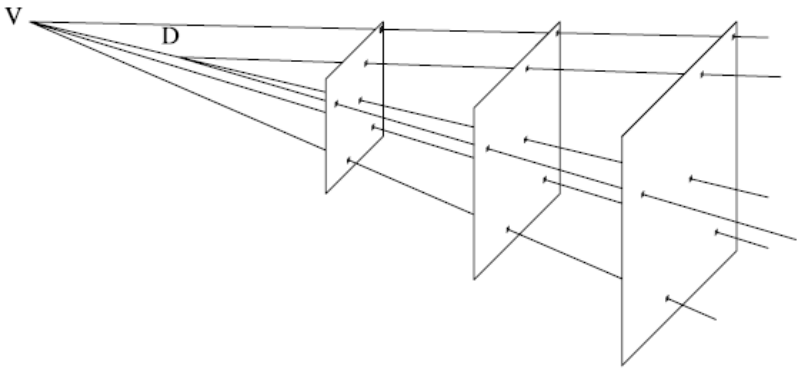

Figure 1.12: Particle track recreation with pixel detectors [4]. Point V is the initial collision vertex and point D is the the point of decay of a resulting particle.

gan in 1993. The campaign resulted in pixel detectors being installed as part of the DELPHI experiment in 1997 [47]. Silicon pixel detectors are now integral parts of the state-of-the-art CMS and ATLAS detectors at the LHC. The inner detector system closest to the collision point is composed of pixel detectors.

Pixel detectors can be made with pixel dimensions down to a few hundred microns a side, providing very precise spatial resolution. This is important in particle colliders which try to detect short lived particles. Figure 1.12 shows how the path of passing particles can be reconstructed. For short lived particles that decay rapidly, the distance between points V and D is on the order of millimeters. Detector requirements are often described in terms of the impact parameter, defined by minimum perpendicular distance of the reconstructed particle path from the vertex V. To accurately distinguish the tracks coming from points V and D, an accuracy of 10 % $c\tau$ is commonly assumed, where c is the speed of light and τ is the particle lifetime [4]. For a particle lifetime of a picosecond, this requires an accuracy of $\leq 30\mu m$. Pixel sizes as low as 100 μm x 150 μm are in use in detectors such as CMS [48] with even smaller pixel sizes being installed in tracking systems, such as the tracker upgrade for the

STAR detector at the Relativistic Heavy Ion Collider (RHIC) where 30 μm x 30 μm pixels named MIMOSA are used [49].

1.6 Hybrid vs. Monolithic Pixel Detectors

In order to gather the information from the sensor, it needs to be connected to the readout electronics. Current state of the art detectors are hybrid detectors, in which the detector and readout electronics are fabricated separately and then bonded together afterwards. The type of bonding depends on the type of detector and is often dictated by mechanical constraints.

Research is now on-going in the fabrication of monolithic detectors in which the electronics and detector are built together on the same substrate. This has the potential to reduce the cost and material budget of future detectors but comes at the cost of more complex processing techniques and added difficulties of controlling the interaction between the detector and electronics.

1.6.1 Hybrid Pixel Detectors

For pad and microstrip detectors, the connection between the detector and electronics can be accomplished with wire bonding. Small wires connect bonding pads on the detector side to bonding pads on the electronics side as shown in Figure 1.13. For microstrip detectors, this requires very precise machining as the distance between strips may only be a few tens of micrometers.

For pixel detectors however, the size and density of the pixels can make wire bonding impractical. Instead, the bump bonding technique is used. Balls of solder are placed at specific sites in each pixel. These are then carefully aligned with pads on the electronics side and the solder balls are remelted to provide the contact as illustrated in Figure 1.14. The

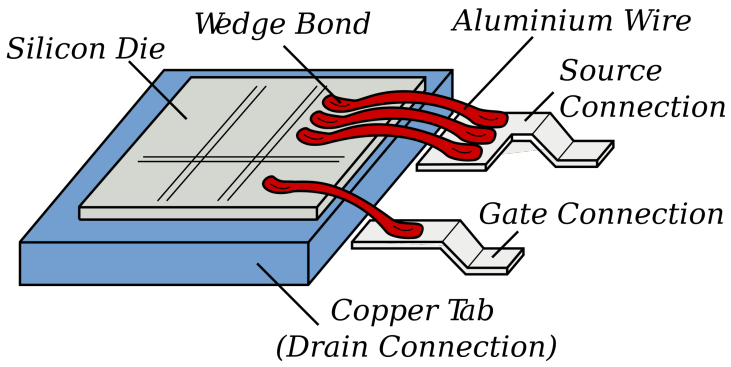

Figure 1.13: Wire Bonding [50]

bump bonds are only a few micrometers in diameter, making placement and proper alignment of the entire grid a complex procedure.

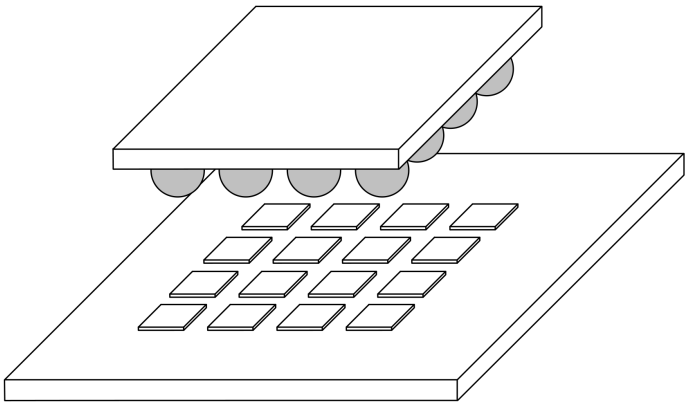

Figure 1.14: Bump Bonding [51]

Hybrid detectors have the advantage of flexible design because the detector and electronics are processed separately. This allows the detector material to be different from the electronics material substrate. For ex-

ample, detector semiconductor material is often of high resistivity while electronics are often developed in low resistivity silicon.

Despite the great advancements made with hybrid detectors, there are some limitations to using hybrid detectors for physics experiments. Due to the use of a sensor and electronics wafer, the minimum thickness of the detector is limited. The minimum pixel size may also be limited by the accuracy of the bump bonding technique. The bump bonding technique itself is a complicated and expensive procedure and may represent the majority of the manufacturing cost of the detector.

1.6.2 Monolithic Detectors

Monolithic detectors have the potential to overcome some of the limitations of hybrid detectors. By creating the sensor and electronics in the same substrate, the thickness of the detector can be reduced. Pixel sizes may be reduced down to tens of microns per side and the expensive step of bump bonding may be avoided all together.

However, to benefit from these advantages, one has to overcome the challenges of building a monolithic detector. Constructing the detector often involves extra non-standard process steps that have to be optimized. Since the sensor and the electronics are now on the same substrate, they may interfere electrically with each other. Placing the electronics close to the detector will also expose the electronics to high levels of radiation. These challenges have to be overcome before the potential of monolithic detectors can be fully realized.

Research in monolithic detectors has been ongoing since the 1990's although large scale applications are only starting to be realized. The Depleted Field Effect Transistor (DEPFET) was proposed in 1987 [52] and later confirmed experimentally in 1990 [53]. The DEPFET is a p-channel MOSFET, below which an n-type bulk is depleted. A potential minimum is created below the transistor channel. As a passing particle creates electron-hole pairs, the holes move toward the back bias while the electrons move toward the potential minimum where they are trapped. The collected charge acts as an internal gate, modulating the transistor

current so that the device acts as both a detector and signal amplifier. Construction of the device requires careful control of the channel limits and internal gate, as well as the addition of a clearing mechanism to periodically remove the collected charge as shown in Figure 1.15. DEPFET based detectors will be used for the future BELLE II detector at KEK in Japan and are being proposed for the future ILC [54].

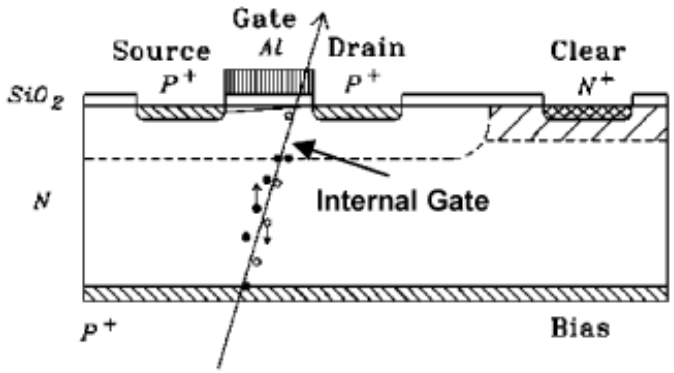

Figure 1.15: DEPFET operation principle [55]

One of the more advanced monolithic detector projects is the MIMOSA series of detectors [56]. These detectors use the epitaxial layer in a CMOS bulk substrate to collect charge. A lightly doped p-epitaxial layer lies between two highly doped p+ layers. An n-well connects to the epitaxial layer to create the sensing diode and collect the charges. One limitation of this technology is that full CMOS circuitry in the active area is not available as only nMOS transistors can be used. Also, the epitaxial layer thickness may only be a few tens of micrometers thick, limiting charge collection.

High Voltage CMOS (HVCMOS) is another technology that is being developed for monolithic detector use. The technology makes use of nested wells to develop monolithic pixels. In particular, the ATLAS collaboration has been studying the technology to create smart diode arrays [57]. A deep n-well in a p-substrate acts as the sensor diode to

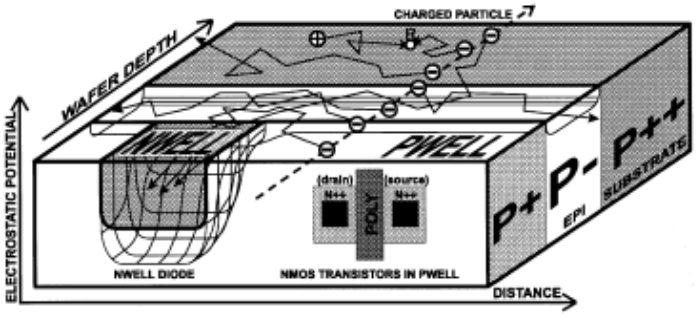

Figure 1.16: MIMOSA epitaxial layer detector [56]

collect charge. A readout circuit can be created directly in the deep n-well: PMOS transistors are created directly in the deep n-well and NMOS transistors are created in a p-well built into the deep n-well. These type of structures can be created in standard substrates however the use of a HVCMOS technology is particularly useful for creating sensors. HVCMOS utilizes substrates with resistivity greater than 10 Ωcm which allows for the application of higher bias voltages and larger depletion zones. With HVCMOS, typical values for the depletion region are 15 μm with applied voltages of 60V.

More recently, advances in Through Silicon Via (TSV) technology are being explored to build 3D silicon detectors [58]. In 3D detectors, the sensors and read out electronics are first developed in separate wafers. Instead of bump bonding the wafers together as in hybrid detectors, the wafers are bonded together and the interconnects are made with through silicon vias. Two wafer are bonded together then a hole is etched between different metal layers present on each wafer. The hole is then filled with metal to create the interconnect.

Another candidate technology being investigated is silicon-on-insulator technology. Silicon-on-insulator technology incorporates two different silicon layers separated by an insulating middle oxide layer. This technology is the basis for the TRAPPISTe series of detectors.

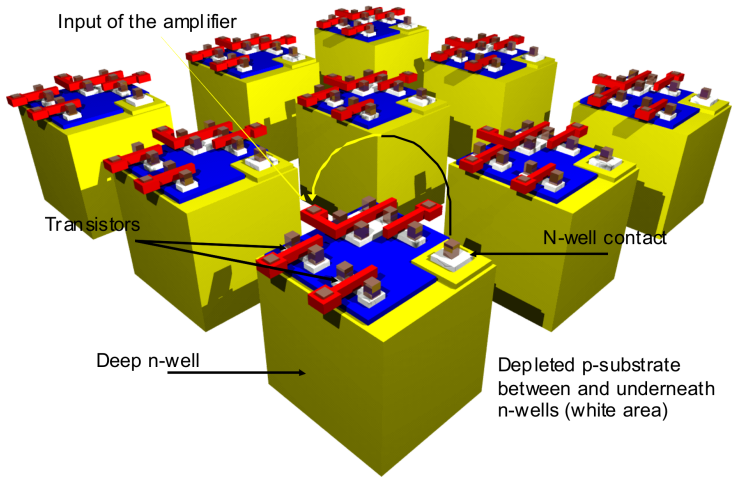

Figure 1.17: HVCMOS pixels with electronics developed in deep n-wells [57]

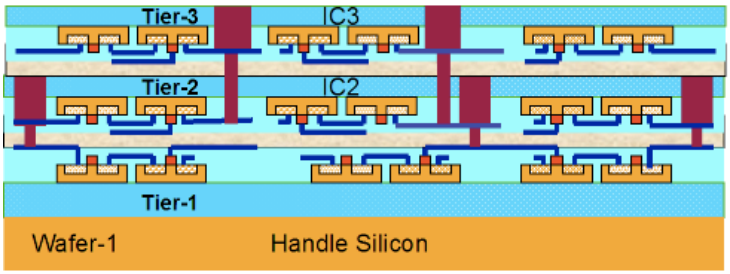

Figure 1.18: Through silicon vias shown in purple creating interconnects between bonded wafers [59]

1.7 Silicon-on-Insulator Technology

The idea of fabricating transistors on a thin semiconductor film has been around for a long time. In fact, the first field-effect transistor patent issued in 1928 was for a device similar to current silicon-on-insulator (SOI) devices, although due to technology limitations there is no evidence this device ever worked [60]. In the 1960's when planar processing technology became available, circuits built on a bulk silicon wafer dominated

the industry although SOI circuits appeared in niche applications such as the military and space industries due to their higher radiation hardness to single event effects. The mass production of SOI circuits occurred in 1998 when IBM decided to use the technology for its PowerPC MPU. Currently, SOI is used in the RF wireless communications industry by companies such as Peregrine, RFMD, and Skyworks with technologies down to $0.13\mu m$ in 2013. ST Microelectronics already has 28nm FD-SOI technology in production for use in low power mobile applications, with 20nm and 14nm FD-SOI technology in development.

1.7.1 SOI Wafer

An SOI wafer consists of a thin top active silicon layer on top of an insulating layer. The top active silicon layer can range from less than ten nanometers to a few hundreds of nanometers thick. The buried oxide (BOX) layer is on the order of a few tens of nanometers thick with advanced processes developing thin buried oxide layers 15nm to 20nm thick. The bottom handle wafer is typically 300-500 μm thick and can be thinned down as required.

The first SOI wafers for large commercial integrated circuit use were produced in 1978 by K. Izumi. His method called SIMOX (Separation by Implanted Oxygen) involves implanting a silicon wafer with a high fluence of oxygen atoms. The wafer is then annealed, allowing a SiO_2 layer to form under a thin silicon layer. The SIMOX method produces high quality wafers but is an expensive process due to the large oxygen implantation.

Another method of SOI production called Smart Cut™was patented by M. Bruel [61]. This method begins with two different wafers. The first wafer is oxidized to created a top insulating layer and then implanted with H+ ions which forms a weakened layer inside the wafer, near the top. The first wafer is then bonded to the second wafer and cleaved along the weakened layer, leaving behind the insulating layer and a thin silicon layer. The process is shown in Figure 1.19 with the resulting SOI wafer comprising the top active layer, middle insulating oxide layer and

bottom handle layer. A wafer formed with this technique is called a UNIBOND™wafer.

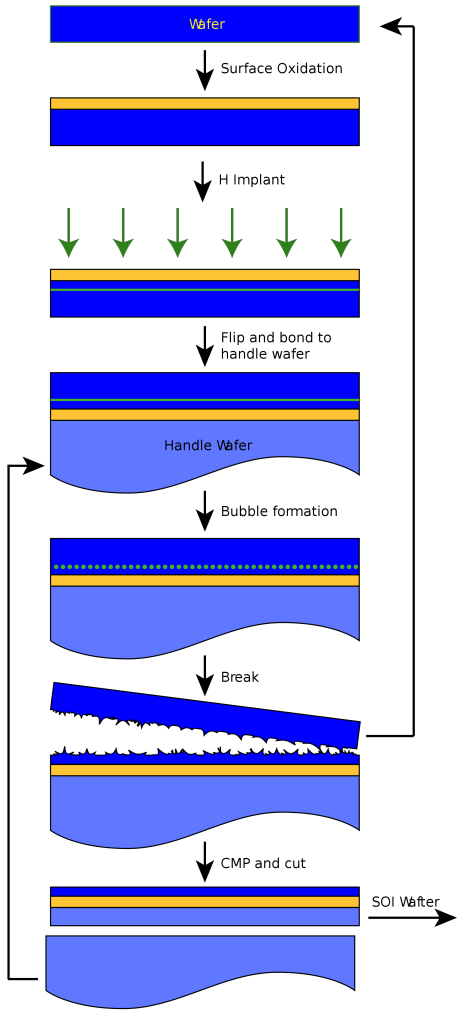

Figure 1.19: Smart Cut SOI wafer process [62]

The UNIBOND™wafer is of particular interest to detector development because the top and bottom silicon layers can be different. In most applications, the bottom layer only acts as a mechanical support for the electronics in the thin top active layer. For detector development, the

bottom handle wafer may be used as the sensor area. Having two different wafers allows the optimization of layers: high resistivity for the sensor layer and low resistivity for the CMOS circuitry layer. These wafers are now available commercially, notably from SOITEC [61] amongst others.

1.7.2 SOI CMOS vs. Bulk CMOS

There are several advantages to using SOI CMOS technology over standard bulk CMOS. As shown in Figures 1.20 and 1.21, in a standard bulk process each transistor is insulated by a well structure with a pn reversed biased diode. In SOI, each transistor is better insulated with an oxide insulator, thereby reducing parasitic effects. For high speed circuits, the capacitive coupling of the source and drain to the bulk substrate may limit performance; in SOI this coupling is reduced by the BOX. The absence of the well structures in SOI enables more compact circuit layout so that more circuitry can be included in the same die area.

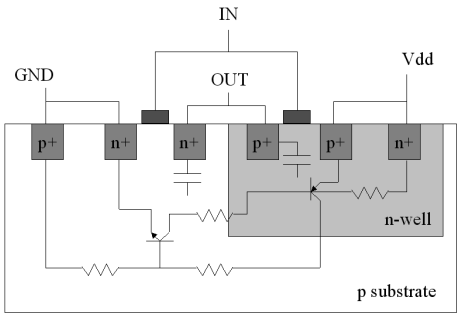

Figure 1.20: Bulk CMOS

In regards to radiation performance, bulk CMOS is known to have parasitic PNPN device in the substrate which may cause latch-ups; this parasitic device does not exist in SOI devices. The thin active layer in SOI devices reduces the amount of charge generated in the active area, making SOI devices less susceptible to single event effects. However, SOI devices may be more susceptible to total ionizing dose (TID) due

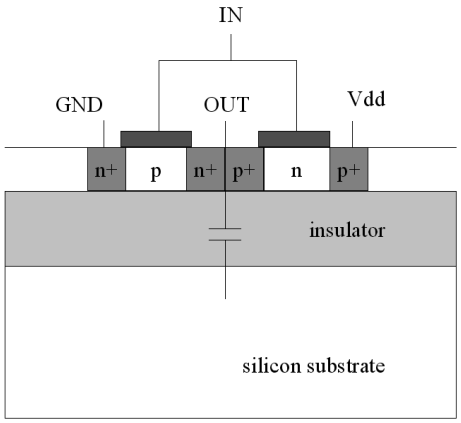

Figure 1.21: SOI CMOS

to the numerous Si and $Si0_2$ interfaces and thick BOX. SOI devices have been shown to withstand up to megarads of radiation. At higher doses however, charge buildup in the BOX can lead to transistor threshold voltage shifts [63]. Radiation tolerance of SOI devices as well as possible mitigation techniques is discussed in Chapter 4.

Two types of SOI transistors exist: partially depleted (PD-SOI) and fully depleted (FD-SOI). PD-SOI has a thicker top active layer (often around 70-200 nm) while the FD-SOI has a thinner active layer (for example, the OKI provided FD-SOI wafer for TRAPPISTe-2 contains a 50 nm top layer). Figure 1.22 illustrates the two. In PD-SOI transistors, a neutral region in the body exists, which can lead to floating body effects such as kink and history effects [64]. While the kink effect increases the drivability of the circuit making it useful for high-speed digital circuits, the body effects are not desirable in analog circuits and require careful design techniques. In FD-SOI, the entire body under the gate is depleted, resulting in significantly reduced body effects. However, the fully depleted body presents more coupling to the buried oxide resulting in more susceptibility to TID effects in the buried oxide. Thick buried oxides present more TID effects but BOX thicknesses are decreasing, down to less than 100nm. In advanced processes, BOX thicknesses close to 10nm are being

studied [65]. The TRAPPISTe line of chips are fabricated in FD-SOI technology.

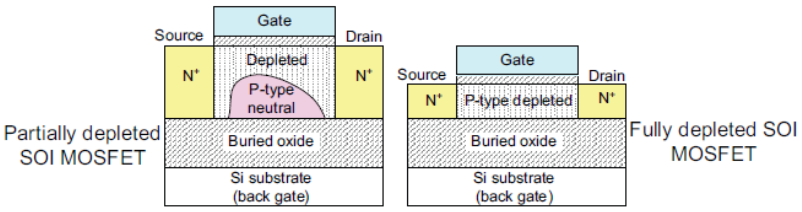

Figure 1.22: Partially depleted and Fully depleted SOI MOSFETs [66]

1.7.3 SOI for Particle Detection

SOI technology can be used to create a particle detector by the realization of a diode in the bottom handle wafer and the integration of the readout electronics in the top active layer. The two parts are separated by the middle oxide layer so that vias are required to connect the two parts, as shown in Figure 1.23. Each layer can be optimized for its intended application; the bottom handle layer for the sensor can be made of high resistivity silicon and the top active layer holding the electronics can be made of lower resistivity silicon. This structure avoids the need for complicated bump bonding procedures.

As a result, the detector and readout electronics may be processed together in one monolithic device. Complications arising from this device include the extra processing steps required to create the diode and through vias. Of particular concern is the backgate effect. In order to operate the detector, the sensor in the bottom layer should be depleted. This requires biasing of the detector where a voltage is applied to the bottom substrate. This voltage generates an electric field throughout the bottom layer which may affect the electronics in the top active layer.

Research in using SOI to build a monolithic detector was first published in 1993 by Diebrickx and others [67]. However, due to limits in SOI wafer

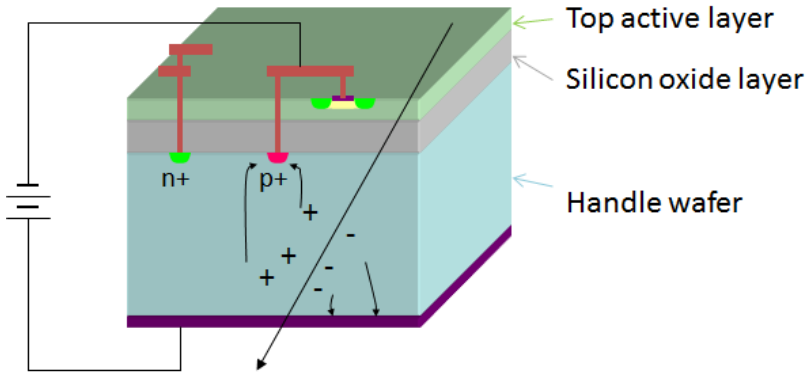

Figure 1.23: SOI wafer used as a monolithic detector. A sensor is created in the bottom handle layer and connected to the readout in the active layer with metal vias.

processing techniques at the time, a complete working detector was not built. In the 2000's, the SUCIMA project has been investigating the use of SOI to build monolithic detectors for medical applications [68]. In 2005, monolithic detector development in SOI technology began at the High Energy Accelerator Research Organization known as KEK in Japan [69]. KEK initiated the SOIPIX collaboration, an international collaboration of research organizations with a common interest of developing pixel detectors in SOI technology. The foundry at OKI Semiconductor based in Japan was used to produce the first prototypes. OKI Semiconductor was acquired by ROHM Semiconductor in 2008 and has since been renamed LAPIS Semiconductor.

In 2006, the first multi-project wafer (MPW) of the SOIPIX collaboration was performed. MPW runs permit several research institutions to share the cost of manufacturing by placing several project layouts on one wafer. The first SOI detectors were developed in $0.15\mu m$ OKI technology [70]. In 2007, the $0.15\mu m$ process line was shut down and pixel development was moved to a $0.2\mu m$ process line. Current SOIPIX participants include institutions such as Fermilab, Lawrence Berkeley National Labs, University of Hawaii, Kyoto University, INP Krakow and others, who have all joined in MPW runs [71]. About two MPW runs are

performed per year. The TRAPPISTe project, started by the Université catholique de Louvain and the Universitat Autònoma de Barcelona, joined the SOIPIX collaboration in 2010.

Pixel sensors developed within the collaboration include INTPIX and CNTPIX developed by KEK, which are based on signal integration and counting type schemes respectively [72], the MAMBO series of detectors developed by Fermi National Laboratories [73] to detect soft X-rays and the SOI-Imager series of devices developed by the SOIPD collaboration [74]. Working with OKI technology within the SOIPIX collaboration, these projects have been developing methods to improve the performance of monolithic SOI detectors. In particular, providing better insulation between the electronics in the active layer and the sensor in the bottom layer. Buried P-well [75] and nested well structures have been developed to shield the readout circuitry from the back gate effect.

1.7.3.1 TRAPPISTe SOI Technology

TRAPPISTe is a research and development project with the aim of studying the feasibility of using SOI technology to develop monolithic particle detectors. In 2009, the first device and test structures for TRAPPISTe-1 were developed at the Université catholique the Louvain's WINFAB facility. In 2010, TRAPPISTe joined the SOIPIX collaboration to develop the TRAPPISTe-2 chip. The SOIPIX collaboration provides access to multi-project wafer runs in OKI Semiconductor (now LAPIS Semiconductor) technology. These two devices use two different technology processes which are summarized in Table 1.3.

The WINFAB technology is a larger feature technology with thicker layer thicknesses and a low resistivity handle wafer. A low resistivity handle wafer is not ideal for detector development as higher depletion voltages are required to deplete the detector. However, this technology was used to construct the first TRAPPISTe-1 amplifier and readout circuits for preliminary tests and methodology development.

	WINFAB	**OKI**
Process	2 μm FD-SOI	0.2 μm FD-SOI
Top Active Layer Thickness	100 nm	50 nm
Buried Oxide Layer Thickness	400 nm	200 nm
Bottom Handle Layer Thickness	$\approx$500 μm	$\approx$300 μm
Handle Layer Type	P-type	N-type
Handle Layer Resistivity	15-25 Ωcm	700 and 10 000 Ωcm
Metal Layers	1	5
Polysilicon Layers	1	1

Table 1.3: Summary of TRAPPISTe process technology properties.

The OKI technology provides a ten times smaller feature size and a high resistivity handle wafer. The smaller feature size and higher number of metal layers allows for higher integration of circuitry. The first TRAPPISTe pixel sensors with integrated amplifiers were produced as part of the TRAPPISTe-2 test device.

1.8 General Readout Electronics

Just as important as the design of the sensor is the design of the readout electronics. The readout electronics converts the charge induced in the sensor into a signal suitable for signal processing. A typical readout chain for a semiconductor detector, as shown in Figure 1.24, consists of a charge amplifier, shaping amplifier and digitizer.

The charge sensitive amplifier (CSA) is an essential first stage of the chain as it converts the charge collected in the sensor into a voltage output. The shaping amplifier then filters and shapes the CSA output into a signal suitable for the digitizer. This could include amplifying the

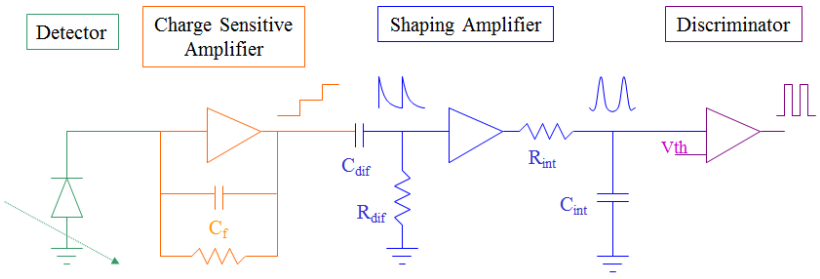

Figure 1.24: Typical readout electronics chain.

signal, filtering the noise of the signal and/or broadening the signal so that the digitizer is able to properly convert the signal into a digital value. The digitizer implementation can range from a simple discriminator with a trigger threshold to a full analog-to-digital converter (ADC).

Current trends in readout electronics are resulting in the miniaturization of the electronics and digital filtering. As technology nodes become smaller, more complex electronics can be placed in smaller areas, proving a higher density of readout channels and more in situ signal processing. Digitization of the signal may now occur earlier in the signal chain as the development of very fast ADCs and signal processors now allow direct digitization of the CSA signal [76]. The role of the shaping amplifier can then be accomplished with digital signal processors.

The design of the CSA is the first step in the readout chain. In general, the CSA is an amplifier configured as an integrator which integrates the current produced in the detector by passing radiation onto a feedback capacitor. It is often a wide bandwidth amplifier in order to react quickly to the fast induced signals.

The CSA needs to be tailored to the specifications of the detector. For example, the expected amount of charge collected in the detector will influence the CSA gain. Another important factor is the capacitance of the detector which influences the noise of the readout system. Detector capacitances can range from tens of picofarads for pad detectors to a few picofarads for strip detectors and down to tens of femtofarads for pixel

detectors. These specifications affect the design of the CSA as detailed in Chapter 2.

1.9 Conclusion

The TRAPPISTe project is a research and development project with the goal of developing a monolithic pixel detector in SOI technology. SOI technology provides several advantages over current state of the art bulk CMOS hybrid detectors. Of particular importance is the elimination of bump bonding between the sensor and readout electronics. Bump bonding is an expensive and technically challenging technique; avoiding it can save a lot of the cost of building large detector systems. Monolithic detectors also reduce the amount of material used as the detector and electronics are all constructed on the same wafer which leads to a reduction in material costs as well as reduced back scattering.

SOI technology also offers advantages over other monolithic technologies. SOI technology is a mature and commercially available technology. While developing a monolithic detector in SOI, it would be possible to exploit this knowledge for rapid development as opposed to technologies which require more specialized techniques such as DEPFETs. SOI technology also has the advantage of full access to circuit development if the circuitry in the top layer can be properly isolated from the sensor layer. Technologies such as epitaxial layer detectors are limited to nMOS transistors; an SOI detector could use full CMOS circuitry to incorporate more advanced readout systems. SOI technology can also be combined with Through Silicon Vias to create 3D circuits to create a monolithic detector with advanced readout circuit capabilities.

While there are many apparent advantages to building a detector in SOI technology, there are also several challenges. While the middle oxide layer provides some isolation between the readout circuitry and sensor layers, there is still be interaction between the them. There is also the issue of radiation hardness. SOI circuits are resistant to single event effects however TID effects can be significant due to the buried oxide layer.

The TRAPPISTe project aims to study these issues and the development of the first proof of concept devices is shown in this thesis.

CHAPTER 2

Charge Amplifier Study

The first part of a typical semiconductor readout chain is a charge sensitive amplifier (CSA). The role of the CSA is to convert the charge generated in the detector into a voltage signal. The CSA output is then further processed by signal filters or digitizers according to the needs of the detector system. As the CSA directly interfaces with the detector, its design depends on the type of detector being used and it plays an important role in determining the gain, noise and speed of the readout system.

This chapter describes a study of a charge sensitive amplifier design. First, relevant detector specifications are discussed as they are important in setting the CSA specifications. Then a top down design methodology of a charge sensitive amplifier is developed. The methodology uses readout specifications and theoretical amplifier equations to aid in sizing the amplifier transistors. The synthesis is based on the g_m/I_D methodology [77], which allows the sizing of transistors based parameters derived from the target process. After an initial transistor sizing

with the methodology, the amplifier is simulated in SPICE and modified as necessary to ensure proper circuit operation.

The CSA in this study was then fabricated in a 2 μm FD-SOI CMOS technology at the WINFAB facility at the Université catholique de Louvain. No detector was attached to the amplifier. However a test charge via a series input capacitor was used to characterize the amplifier under controlled conditions. The backplane of the die was also biased to observe the amplifier response to an applied back voltage. The amplifier was electrically characterized and the measurements were compared to the expected results to validate the design methodology.

2.1 Detector Specifications

In order to design the front-end amplifier, one needs to know the characteristics of the detector it will interface to. The first important piece of information is the amount of charge that is expected to be collected in the detector. The amount of charge collected is used to set the gain of the CSA and to determine the resolution of the detector readout. For particle physics tracking detectors, one can expect that a minimizing ionizing particle (MIP) will deposit around 60-80 electrons per micrometer of silicon thickness. A typical detector thickness for tracking detectors is $300\mu m$ therefore passing particles generate approximately 24000 electrons in the detector bulk.

The reverse bias current of the semiconductor detector is an important factor in determining the noise of the readout electronics. Even in the absence of passing radiation, a biased semiconductor detector exhibits a leakage current that contributes to the noise of the system, as will be shown. The physical layout constraints of the readout also need to be taken into consideration. Several amplifiers may be required to be placed in a small area to interface to multiple channels of a strip or pixel detector, leading to tight restrictions on the layout area.

Of particular importance to the noise performance is the capacitance. It can be shown that the input capacitance of the CSA can be chosen

to minimize the output noise of the readout chain for a given detector capacitance. The capacitance of a silicon detector can be calculated from its geometry.

2.1.1 Microstrip Detector Capacitance

A microstrip detector is comprised of long and thin implants laid out parallel to each other on a semiconductor bulk. The capacitance of each strip C_d depends on the geometry of the detector: the detector thickness (d), the strip pitch (p) and strip width (w). Figure 2.1 illustrates the geometrical parameters of a microstrip detector.

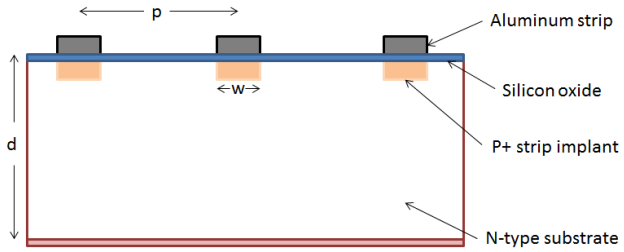

Figure 2.1: Cross-section of a microstrip detector: d is detector thickness, p is strip pitch and w is strip width.

The total capacitance of a microstrip detector can be approximated by summing two capacitance quantities: the backplane capacitance C_{back} and the interstrip capacitance C_{inter}. These capacitances can be calculated analytically as shown by Braibant et al. and reproduced here [78].

The backplane capacitance is the capacitance between the strip and the metal backplane. For a fully depleted detector, the capacitance C'_{back} per unit length can be calculated as:

$$C'_{back} = \epsilon_o \epsilon_{si} \frac{p}{d + pf(\frac{w}{p})} \tag{2.1}$$

where ϵ_o is the permittivity of free space, ϵ_{si} is the relative dielectric constant of silicon, d is the thickness of the detector, p is the pitch between

strips and w is the width of each strip. The function f is a universal function derived semi-analytically from Poisson's equations [79]. It describes how a finite width and pitch increases the depletion voltage and decreases the body capacitance. The function is numerically approximated by:

$$f(x) = -0.0011x^{-2} + 0.0586x^{-1} + 0.240 - 0.651x + 0.355x^2 \quad (2.2)$$

The interstrip capacitance is the capacitance between a given strip and neighboring strips and usually dominates the total capacitance. For 0.10 $<$ w/p $<$ 0.55, the interstrip capacitance per unit length can be approximated for an infinitely thick detector to be:

$$C'_{inter,d\to\infty} \approx (0.8 + 1.9\frac{w}{p}) \text{ pF/cm} \quad (2.3)$$

For a finite thickness detector, C_{inter} will be less than the calculated infinite thickness value as the volume of the dielectric is reduced.

Example Microstrip Capacitance Calculation with CMS Detectors

For this amplifier study, CMS microstrip detectors were chosen as representative detectors as their characteristics are well known, having been previously tested at UCL. The strips are 300 μm thick n-type silicon detectors. Two types of microstrips were available with different geometries:

- 7cm long with a pitch of 80μm and a strip width of 20μm
- 2cm long with a pitch of 120μm and a strip width of 30μm

The electrical specifications for the microstrips are listed below and can be found in the CMS Tracker Technical Design Report [37].

- Breakdown voltage: $V_{breakdown} > 500V$
- Leakage current $I_{leakage}$ for single strip $< 500pA$
- Maximum interstrip capacitance: $< 1.3pF/cm$

For these microstrip detectors, w/p is 0.25 giving $f(x) = 0.316$. For the 2cm strips, this results in a C_{back} of $0.367pF/cm$. For the 7cm strips, C_{back} is calculated to be of $0.254pF/cm$

As the maximum interstrip capacitance is known to be $< 1.3pF/cm$, a maximum total capacitance can be calculated. The maximum total capacitance for a 2cm strip can then be calculated to be: $(1.3pF/cm + 0.367pF/cm) \times 2cm = 3.33pF$. For a 7cm strip, the maximum total capacitance is: $(1.3pF/cm + 0.254pF/cm) \times 7cm = 10.9pF$.

2.1.2 Pixel Detector Capacitance

While microstrip detector characteristics were chosen for this particular amplifier study, future TRAPPISTe devices will consist of pixel detectors. As with microstrip detectors, the total capacitance of a pixel depends on the geometry of the pixel implant and is a combination of the backplane capacitance and the inter-pixel capacitances. Analytical expressions to calculate pixel capacitances are presented in a paper from Cerdeira [80] and they are shown in this section.

Figure 2.2 shows the cross-section of a pixel detector, with L as the size of the detector implant, S the distance between the pixel implants and W the depletion width approximated by

$$W \approx \sqrt{2\epsilon_s \mu \rho} \tag{2.4}$$

where ϵ_s is the dielectric constant of silicon, μ is the mobility of the majority carrier and ρ is the resistivity of the detector substrate.

The total capacitance is not only due to the backplane capacitance C_0 but one must also take into account the inter-pixel capacitances. Figure 2.3 shows a top view of a pixel matrix, where the inter-pixel capacitances C_1 (the capacitance between directly adjacent pixels) and C_2 (the capacitance between diagonally adjacent pixels) are shown.

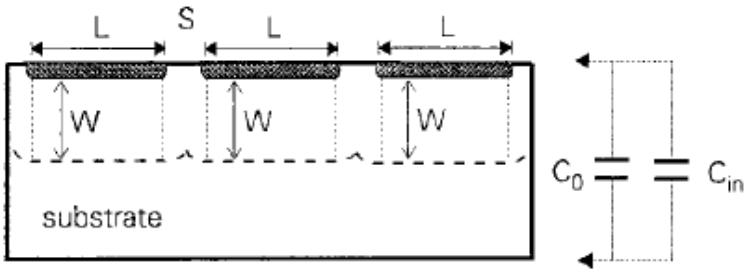

Figure 2.2: Cross-section of a pixel detector showing geometric parameters. [80]

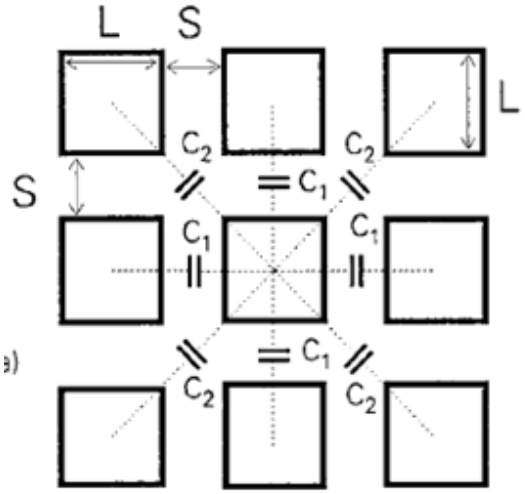

Figure 2.3: Top view of pixel capacitances showing inter-pixel capacitances between adjacent (C_1) and diagonal pixels (C_2). [80]

The total capacitance of a given pixel C_P is a combination of C_0, C_1 and C_2. The calculation of the capacitance can be divided into two cases: when the pixels are virtually grounded and when the pixels are floating. In both cases, the total pixel capacitance calculations are normalized to the ideal one dimensional case:

$$C_{1D} = \frac{\epsilon_s L^2}{W} \tag{2.5}$$

Virtually Grounded Pixels

In the case where the pixels are virtually grounded at the input of the charge amplifier, the total pixel capacitance is the sum of all the capacitance components

$$C_P = C_0 + 4C_1 + 4C_2 \tag{2.6}$$

The capacitance components can be calculated by the following equations derived analytically in the Cerdeira paper [80], where $s = S/W$ and $\lambda = L/W$:

$$\frac{C_0}{C_{1D}} = (1.15)^{(1/\lambda)} + \frac{2.3}{\lambda}\left(1 - e^{-s/\sqrt{\lambda}}\right) \tag{2.7}$$

$$\frac{C_1}{C_{1D}} = \frac{0.23}{s + 0.18}\left(\frac{1}{\lambda}\right)^{0.75} - 0.07\left(\frac{1}{\lambda}\right) \tag{2.8}$$

$$\frac{C_2}{C_{1D}} = 0.1^{\lambda}[1 - 1.15\left(\frac{7}{s+3} - 1\right)s] \tag{2.9}$$

Floating Pixels

In the case where all surrounding pixels are floating, a more complex formulation is required and the input capacitance C_{in} of the CSA must also be taken into account. The total capacitance may be calculated by the following analytically derived equations, where C_0, C_1 and C_2 are the values obtained in the grounded pixel calculations [80]:

$$\frac{C_P}{C_{1D}} = \frac{2}{3}(b^2 + 3c)^{1/2}\cos\frac{\varphi}{3} + \frac{b}{3} \tag{2.10}$$

$$C_0' = C_0 + C_{in} \tag{2.11}$$

$$b = C_0^{'} + 2C_1 + 2C_2 \tag{2.12}$$

$$c = 12C_1C_2 + 2C_0^{'}(C_1 + C_2) \tag{2.13}$$

$$d = 4C_0^{'}C_1C_2 \tag{2.14}$$

$$\cos\varphi = \frac{b^3 + \frac{9}{2}bc + \frac{27}{2}d}{b^2 + 3c}^{3/2} \tag{2.15}$$

Example Pixel Capacitance with UCL Technology

An example calculation for pixel capacitance was performed using specifications of the wafers provided for the UCL 2 μm FD-SOI process. The handle wafer resistivity is $\approx 25\Omega cm$ and a representative value for an input transistor capacitance is taken to be 2fF. A calculation was performed for pixels developed in the TRAPPISTe-1 (see Chapter 3). The matrix is composed of pixels whose total area is 300 μm x 300 μm. In the center of each pixel an N+ implant of size 60 μm x 60 μm is created into the P-type substrate. The pixel parameters for this geometry are then L = 60 μm and S = 240 μm.

Figure 2.4 shows the resulting pixel capacitance for the virtually grounded and floating pixel case. The capacitance starts at 250fF and decreases as the depletion voltage increases to about 50fF at 40V depletion voltage. The virtually grounded and floating capacitances are almost identical in this case as for this geometry and wafer resistance, the C_0 component dominates the total capacitance. While the C_0 component is in the tens of picofarad range, the C_1 and C_2 components are less than 1fF.

Example Pixel Capacitance with OKI Technology

Pixel capacitance calculations were also made for OKI technology parameters. The calculation was done for a 150 $\mu m\times$ 150 μm pixel with

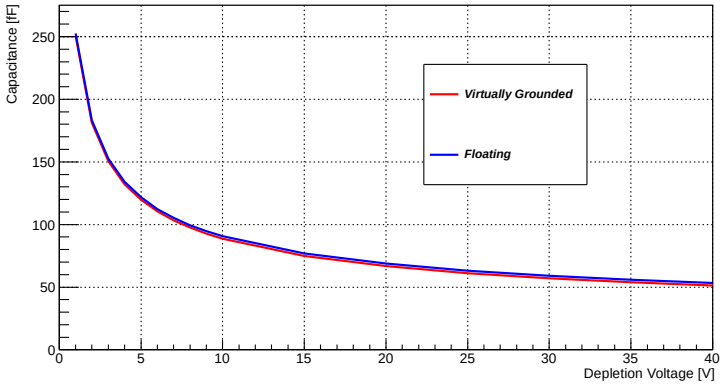

Figure 2.4: Calculated pixel capacitance for a 300 μm x 300 μm pixel in UCL technology

30 μm x 30 μm implants, as implemented in the TRAPPISTe-2 matrices (see Chapter 3). This matrix results in pixel parameters of L = 30 μm and S = 120 μm. OKI provided handle wafers with resistivities of 700 Ωcm and 10 000 Ωcm. The calculated capacitances are plotted in Figure 2.5. Due to the higher resistivity wafers and smaller pixel size, the TRAPPISTe-2 pixel capacitance is lower than TRAPPISTe-1, down to around 10fF at 40V depletion voltage.

A plot of the different components of the capacitance for the 10 000 Ωcm resistivity wafer with grounded pixels is shown in Figure 2.6. In the TRAPPISTe-1 case, the inter-pixel capacitances C_1 and C_2 are relatively insignificant compared than the backplane capacitance C_0 due to the large pixel sizes and low resistivity. For the TRAPPISTe-2 case, the inter-pixel capacitances play a more important role. For example, at 40V back voltage, $C_0 = 6.3fF$, $C_1 = 0.51fF$ and $C_2 = 0.12fF$. The total inter-pixel capacitance is $4C_1 + 4C_2 = 2.52fF$ which is more than a quarter of the total capacitance.

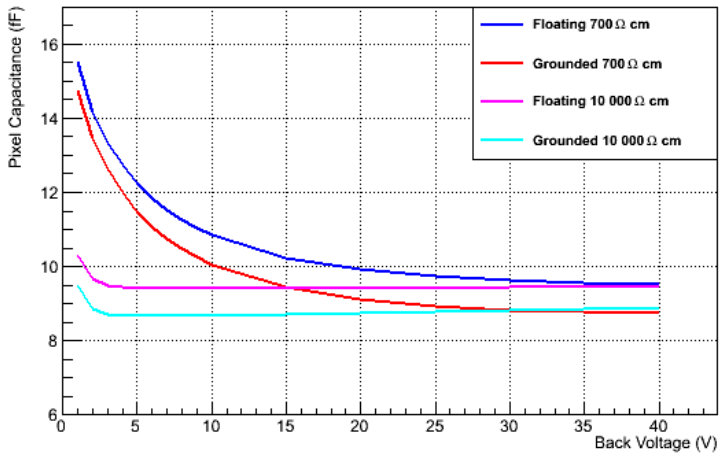

Figure 2.5: Calculated pixel capacitance for a 150 $\mu m\times$ 150 μm pixel in OKI technology.

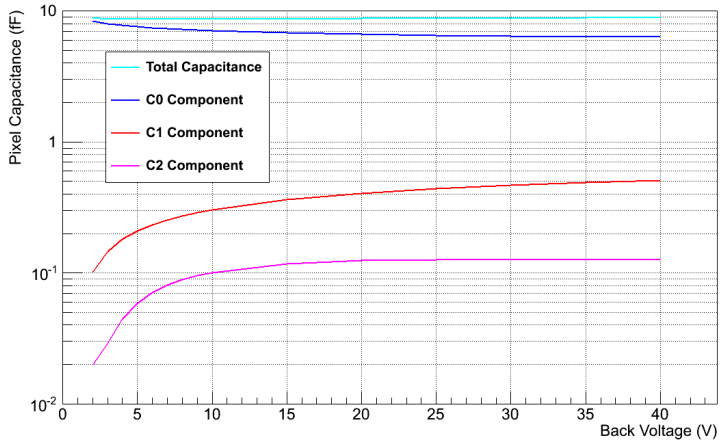

Figure 2.6: Calculated pixel capacitance components for a 150 $\mu m\times$ 150 μm pixel in OKI technology with a 10 kΩcm resistivity and grounded surrounding pixels.

2.2 Charge Sensitive Amplifier Theory

The charge sensitive amplifier (CSA) is often the first stage of a silicon detector readout system (Fig. 2.7). The role of the CSA is to convert the

charge generated in a detector into a voltage signal. This is traditionally accomplished by integrating the charge onto a feedback capacitor C_f. The output of the CSA is typically a step function with amplitude proportional to the input charge. A feedback resistor R_f allows for the discharge of the capacitor to avoid buildup of the output voltage from successive integrations. The output of the CSA is then subsequently filtered and shaped by shaping amplifiers. A standard shaping chain contains a high pass filter followed by one or more low pass filters resulting in a band pass filter to filter out noise. The shaping amplifiers may also amplify the signal if required. The filtered signal then undergoes pulse processing which usually involves digitization with ADCs for further computer processing.

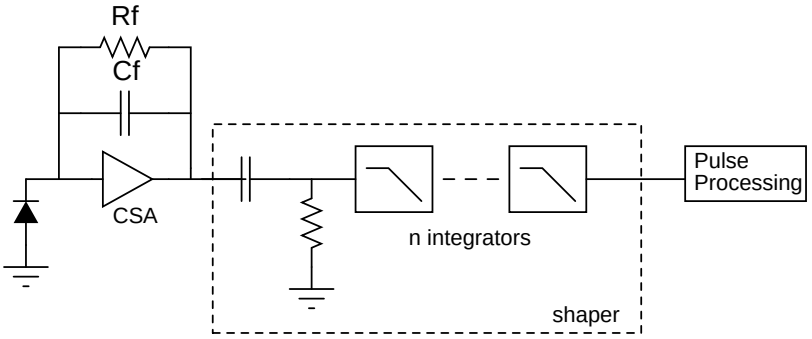

Figure 2.7: A typical front end electronics chain with charge sensitive amplifier, shaper amplifier and pulse processing.

2.2.1 Transfer function

For detector front-end electronics, an operational transconductance amplifier is the standard choice. It provides high gain and low input capacitance, as well as a large bandwidth to accommodate fast input signals. If it is assumed that the amplifier is an operational transconductance amplifier (OTA) with transconductance g_m and output impedance of a parallel load resistor and load capacitor $R_L//C_L$, the transfer function

from the input current signal I_{in} to the voltage output V_{out} can be shown to be [81]:

$$\frac{V_{out}(s)}{I_{in}(s)} = -\frac{g_m}{g_m/R_f + sg_mC_f + s^2C_t(C_f + C_L)} \tag{2.16}$$

where C_t is the total capacitance at the input of the CSA including detector capacitance C_d, parasitic capacitance C_p, feedback capacitance C_f and the input capacitance of the amplifier. The equation holds assuming $g_mR_L >> 1$ and $g_mR_f >> 1$, which in practice is always satisfied as the output impedance for an OTA is high as is the value of the feedback resistor R_F.

Assuming that the poles of equation 2.16 are far apart to ensure stability, they are given by:

$$p_1 = \frac{1}{2\pi\tau_1} = \frac{1}{2\pi R_fC_f} \tag{2.17}$$

$$p_2 = \frac{1}{2\pi\tau_2} = \frac{g_mC_f}{2\pi C_t(C_L + Cf)} = \frac{GBWC_f}{C_t} \tag{2.18}$$

where GBW is the gain bandwidth product of the OTA.

The resulting output of the CSA in the time domain is governed by the time constants τ_1 and τ_2 from equations 2.17 and 2.18 respectively, given by:

$$V_{out}(t) = \frac{Q\tau_1}{C_f\,(\tau_1 - \tau_2)}\left(e^{-t/\tau_1} - e^{-t/\tau_2}\right) \tag{2.19}$$

where Q is the charge input obtained by the integral of the current input signal I_{in}. In general, $\tau_2 \ll \tau_1$ so that the output is an exponential step function with a risetime t_r from 10% to 90% of the amplitude equal to:

$$t_r = 2.2\tau_2 = 2.2\frac{C_t}{2\pi GBWC_f} \tag{2.20}$$

2.2.2 Noise

The noise output of the amplifying chain can be broken down in three sources: thermal noise, 1/f noise and leakage current noise. These can be calculated with Equations 2.21, 2.22 and 2.23. These equations are shown by Chang [81], where k is the Boltzmann constant, T is the temperature, τ_S is the shaping time of the shaper amplifier, n is the order of the shaper filter equal to the number of low pass filters, I_o is the detector leakage current and B is the mathematical beta function defined by $B(x,y) = \int_0^1 t^{x-1}(1-t)^{y-1}\,dt$. The noise is generally specified as total equivalent noise charge (ENC) which is defined as the rms noise at the amplifier chain output expressed in electrons input charge.

Thermal noise

The thermal noise ENC_d is associated with the channel resistance of the input MOSFET and is given below for a MOSFET in saturation. One can see that increasing the transistor g_m and decreasing the input capacitance lowers the overall thermal noise.

$$ENC_d^2 = \frac{8}{3}kT\frac{1}{g_m}\frac{C_t^2 B(\frac{3}{2}, n-\frac{1}{2})n}{q^2 4\pi\tau_s}\frac{n!^2 e^{2n}}{n^{2n}} \tag{2.21}$$

Flicker noise

The flicker noise ENC_f, also known as 1/f noise, is a frequency dependent noise seen in MOS devices attributed to fluctuations in conductivity. It can be calculated from the flicker noise constant K_f which is a device and technology dependent parameter, the gate oxide capacitance per unit area C_{ox} and the input transistor width (W) and length (L). One can see that the flicker noise is dependent on the process technology and choice of input transistor.

$$ENC_f^2 = \frac{K_f}{C_{ox}^2 WL}\frac{C_t^2}{q^2 2n}\frac{n!^2 e^{2n}}{n^{2n}} \tag{2.22}$$

Leakage current noise

Even in the absence of incident radiation, a detector exhibits a reverse biased current called a leakage or dark current. This leakage current contributes a leakage current noise ENC_0 to the total output noise of the system. It is governed by the peaking time and order of the shaper and therefore independent of the CSA parameters.

$$ENC_0^2 = 2qI_0 \frac{\tau_S B(\frac{1}{2}, n+\frac{1}{2})}{q^2 4\pi n} \frac{n!^2 e^{2n}}{n^{2n}} \tag{2.23}$$

An analysis of these equations shows that the thermal and 1/f noise are dependent on the area W*L of the input transistor. This is due to the dependence on the total input capacitance C_t at the CSA input which includes the capacitance of the input transistor.

Example noise curve

An example noise curve was plotted to illustrate the dependence on the input transistor size on the total noise of the readout. Using the CMS microstrip detectors as an example, the detector leakage current was set to 500pA and the capacitance was chosen to be 5pF (in between the 3pF and 10pF calculated for the two types of microstrips). The process parameters chosen were based on the UCL $2\mu m$ technology with $K_f = 5 \times 10^{-31}\ C^2/cm^2$ and $C_{ox} = 1.1 \times 10^{-15}\ F/\mu m^2$.

The amplifier based parameters were set according to specifications of the amplifier fabricated in this study which will be described in the next section. These amplifier specifications are a feedback capacitor $C_f = 0.2pF$ and a $g_m = 0.4mS$. The shaping time was taken to be $1\mu s$ and an order n=1 filter was set. Plotting equations 2.21, 2.22 and 2.23 as a function of the input transistor area results in Figure 2.8. One can see the dependence of the flicker and thermal noise on the transistor area and that the leakage current noise is independent of the transistor area. The calculated optimal area is around 1000 μm^2.

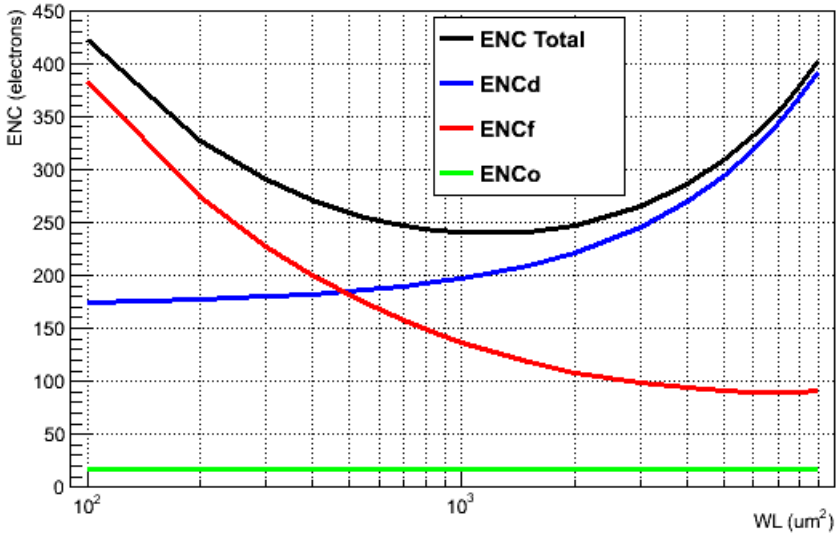

Figure 2.8: ENC vs Input Transistor Area in WINFAB technology using CMS microstrip characteristics.

2.3 CSA Synthesis with g_m/I_D Methodology

In order to facilitate the design of the CSA, a top-down g_m/I_D methodology was developed as the starting point in the design. The methodology starts with the desired amplifier specifications such as the gain and bandwidth to determine the g_m and bias currents of the amplifier transistors. g_m/I_D curves can then be used to select transistor sizes.

The ratio of a transistor transconductance to its drain current g_m/I_D is a key parameter that can be used to characterize transistor performance and aid in design synthesis [77]. Using the EKV transistor model, it can be shown that for a long channel MOSFET in saturation [82]:

$$g_m/I_D = \frac{1}{nU_T}\frac{1-e^{-\sqrt{(IC)}}}{\sqrt{(IC)}} \tag{2.24}$$

where U_T is the thermal potential equal to 26mV at room temperature. IC is an adimensional number given by:

$$IC = \frac{I_D}{2n\mu C_{ox}\frac{W}{L}U_T^2} \tag{2.25}$$

where n, μ and C_{ox} are the linearized body effect, the inversion layer minority carrier mobility and the gate oxide capacitance per unit area respectively. These are all technological parameters fixed by the fabrication process.

From equations 2.24 and 2.25, one can see that to the first order the parameter g_m/I_D as a function of the normalized current $I' = I_D/(W/L)$ only depends on technological parameters. So for a given fabrication process, this parameter serves as a universal characteristic for all transistors of similar types, ie. nMOS or pMOS. The g_m/I_D reflects the efficiency of the transistor to amplify a signal and to transform a static current into a dynamic transconductance and, as a result, the gain-bandwidth product for a given current.

The use of the g_m/I_D formulation allows one to estimate an important design parameter: the W/L of a transistor. g_m/I_D values fall within a limited range of known values; at room temperature, values for MOS transistors are constrained between 0 and 38 V^{-1}. In practical cases, acceptable values are limited by desired specifications and an initial guess can be conveniently made. As the g_m/I_D does not depend on transistor size and is linked to the normalized current $I' = I_D/(W/L)$, choosing a g_m/I_D value and desired bias current leads to the determination of transistor size.

Figure 2.9 shows the g_m/I_D plot for a standard voltage threshold nMOS transistor in the UCL 2.0μm FD-SOI CMOS process.

Starting from amplifier specifications and using the g_m/I_D plots for a given process, one can create a top-down synthesis of an amplifier.

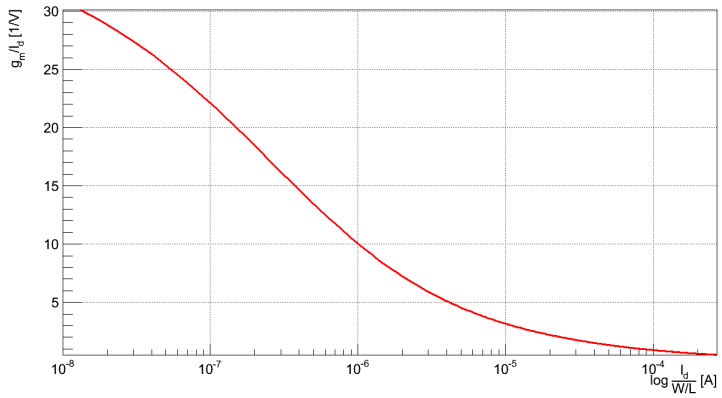

Figure 2.9: g_m/I_D vs normalized drain current for an nMOS transistor in the UCL 2.0 μm process

2.3.1 Cascode Core Architecture

A standard amplifier architecture for charge sensitive amplifiers is a folded cascode. Using a folded cascode arrangement, as shown by transistors M1 and M3 in Figure 2.10, a low number of stages can be implemented to minimize power consumption [83]. Transistor M4 acts as a current source.

The transconductance of the amplifier is given by the g_{m1} of the input transistor M1. The node connecting M1 and M3 is of interest as its capacitance determines the position of the non-dominant pole. The capacitance at that node, hereafter referred to as C_2, consists of the gate-to-source capacitance of M3 (C_{GS3}), the drain-to-bulk capacitance of M1 (C_{DB1}), the gate-to-drain capacitance of M1 (C_{GD1}), as well as the gate-to-drain capacitance of M2 (C_{GD2}). The non-dominant pole p_{nd} is located at g_{m3}/C_2.

The full architecture of the amplifier in this study is shown in Figure 2.11. It is a single-ended input and single-ended output amplifier. The input signal from the detector is labeled as node IN and the output signal is read out from node OUT. External applied biases are the amplifier bias

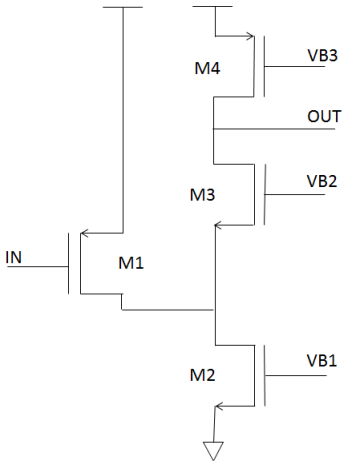

Figure 2.10: Folded cascode core of the CSA.

voltage V_{dd}, amplifier bias current ICSA and feedback transistor voltage V_{rf}. For the amplifier developed in UCL technology, V_{dd} is 2.5V. The bias current ICSA and feedback transistor voltage V_{rf} can be varied to tune the amplifier performance. The amplifier consists of transistors M1-M4 comprising the cascode core and transistors M5-M8 which are used to bias the core transistors. The feedback consists of the feedback capacitor C_f which integrates the charge and a feedback resistance to provide DC stability. The feedback resistance is implemented as a long and thin nMOS transistor MF (W/L of 3 μm/30 μm in this case) [84].

2.3.2 Transistor Sizing with g_m/I_D

The sizing of the CSA transistors is determined by the amplifier requirements and detector specifications. The detector specifications chosen for this study were based on the CMS microstrips. The sizing methodology is illustrated in Figure 2.12 with the specific values for the sizing detailed below.

The starting point of the synthesis is the charge-to-voltage gain of the amplifier which is set by the feedback capacitor C_f. In this study, a C_f

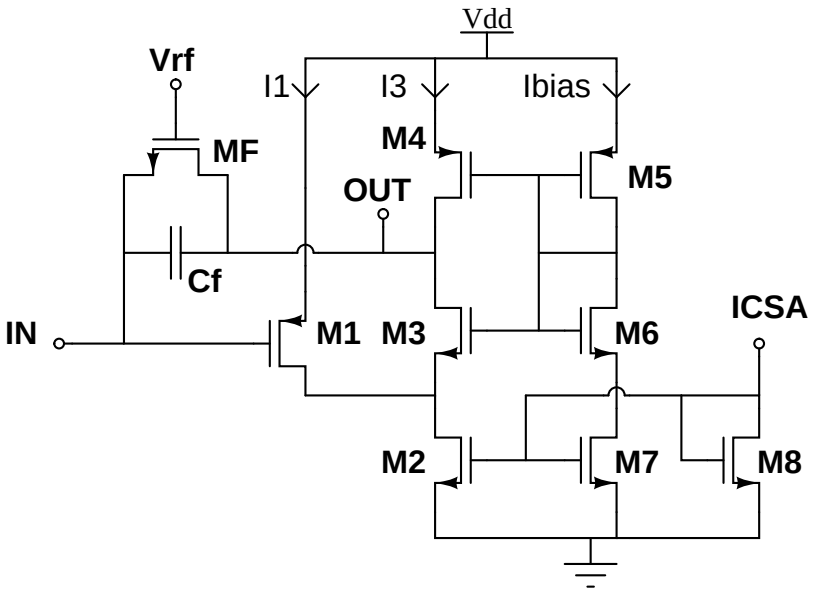

Figure 2.11: Full CSA architecture with cascode core and biasing transistors.

of 0.2pF was chosen as the size of the capacitor fit comfortably within the layout area. For a charge Q of 1 MIP equal to 24000 electrons (valid for a 300 μm thick detector), the gain of the system is calculated to be:

$$V = Q/C_f = \frac{1.6 \times 10^{-19} \times 24000}{0.2 \times 10^{-12}} \approx 18mV/MIP \tag{2.26}$$

An example detector capacitance of 5pF was selected as this lies between the 3pF and 10pF values calculated for the microstrip detectors. The total input capacitance can be estimated to be:

$$C_T = C_D + C_f = 5.2pF \tag{2.27}$$

The response of the amplifier should be quick to respond to the fast charge generation of a passing particle. For a standard signal risetime t_r of 100 ns, the desired gain bandwidth can be calculated from equation

2.20 to be:

$$GBW = 2.2\frac{C_T/C_f}{2\pi t_r} = 91MHz \tag{2.28}$$

From the GBW, the transconductance of the input transistor g_{m1} for an example load capacitance $C_L = 0.1pF$ is calculated from equation 2.18 to be:

$$g_{m1} = 2\pi GBW(C_L + C_f) = 0.4mS \tag{2.29}$$

The two poles from equations 2.17 and 2.18 are found at:

$$p_1 = 1/2\pi R_f C_f = 7958Hz \text{ (for } R_f = 100 \text{ M}\Omega) \tag{2.30}$$

$$p_2 = \frac{GBW}{C_T/C_f} = 3.5MHz \tag{2.31}$$

Using the g_m/I_D curves and the amplifier specifications, it is possible to size the different transistors. The sizing process is shown schematically in Figure 2.12. First, the amplifier g_{m1}, GBW and main poles p_1 and p_2 are calculated from equations 2.28 to 2.31. The input transistor M1 is the first to be sized. Its transconductance g_{m1} is known and by selecting a g_m/I_D value, the input transistor drain current and size (W/L) can be determined. To facilitate the study, initial g_m/I_D values were set to match the values in the text by Chang [81] and then modified as required. The length L of the transistors for the core of the amplifier were chosen to be the smallest length available in the given technology in order to reduce the layout size. For the UCL technology, the smallest length is $2\mu m$. The length of the bias and current mirror transistors were chosen to be slightly larger to allow for better transistor matching. With the size of the input transistor determined, a check of the expected ENC noise can be made as the noise is dependent on the input transistor size.

The sizing of the other transistors follows from the sizing of the input transistor. From the current I1 passing through the input transistor, the currents I3 and Ibias in the other two branches of the amplifier

(see Figure 2.11) can be chosen by selecting the ratios between I1/I3 and I3/Ibias. For this study, ratios of I1/I3=4 and I3/Ibias=3, as in a paper by Hu [84]. With the current I3, the cascode transistor M3 can be sized, leading to the determination of the parasitic capacitance C_2 at the cascode node. A check can then be made to verify that the non-dominant pole p_{nd} is far from the main poles p_1 and p_2. The sizes of the other biasing transistors are then determined from their bias current and g_m/I_D values.

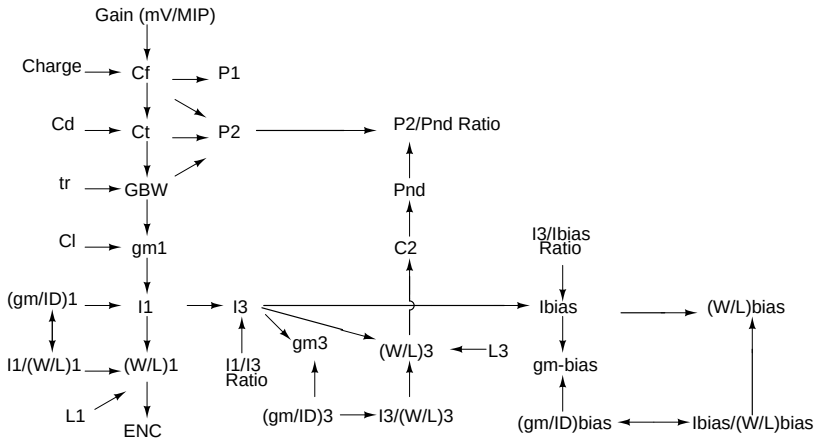

Figure 2.12: Transistor sizing flow diagram. Input transistor denoted by subscript '1', cascode transistor denoted by subscript '3', bias transistors denoted by subscript 'bias'.

The sizing flow provides a good starting point to the design of the amplifier. A script written in MATLAB based on the design flow can generate initial transistor sizes. For this study, the input parameters to the script were the ones shown in this section, Equations 2.26 to 2.31. Using these initial transistor sizes, the amplifier is then simulated in ELDO SPICE to ensure proper operation of the circuit. Transistor sizes are then modified to optimize circuit performance. The resulting transistor sizes for the amplifier in this study (see Figure 2.11 for transistor references) are shown in Table 2.1. The feedback resistor MF was chosen to be a long and thin nMOS, $3\mu m/30\ \mu m$. This size transistor fit comfortably in

the layout and the long and thin nMOS should provide a large feedback resistance.

Transistor	g_m/I_D	W/L [$\mu m/\mu m$]
M1	19.2	200/3
M2	5.3	30/4
M3	6.8	30/4
M4	4.7	44/10
M5	4.7	44/10
M6	4.9	18/4
M7	5.3	24/4
M8	5.3	24/4

Table 2.1: Transistor Dimensions

2.3.3 ELDO SPICE Simulation Results

The CSA was then simulated in ELDO SPICE with transistor models provided by WINFAB. A transient response plot in Figure 2.14 shows the CSA output voltage in response to an input of 24000 electrons (equivalent to the charge generated by 1MIP in $300\mu m$ of silicon). The amplifier was biased with the nominal parameters used during the amplifier design: a VDD of 2.5V and a bias current of $100\mu A$. The feedback resistor was simulated with a high value real resistor set at 100GΩ as shown in the simplified configuration of Figure 2.13 since the SPICE simulator had trouble to properly simulate a feedback transistor. The charge injected at the amplifier input is simulated by a current source with a pulse width of 2.5ns and pulse height of 1.55μA as illustrated in Figure 2.13. The short pulse width represents a quick generation of charge as is expected when a particle passes through a detector and the current of 1.55μA over 2.5ns is equal to a charge injection of 24000 electrons. The detector capacitance C_{DET} was set to 5pF (the calculated microstrip capacitance) and the output capacitance was set to 0.1pF. An output capacitance of 0.1pF as this was expected to be representative of the input capacitance of a shaper amplifier, which would be the second stage of a readout chain.

At each charge injection, the output displays a rapid change in voltage of about 18 mV as expected as is the falltime of 100 ns. The V_{out}/I_{in} AC response was also simulated for a load capacitance of 0.1pF as shown in Figures 2.15 and 2.16. The bandwidth of 40MHz is lower than the expected 91MHz and the phase margin is about 40 degrees. The AC response is dependent on the load capacitance with larger capacitances raising the phase margin but lowering the bandwidth.

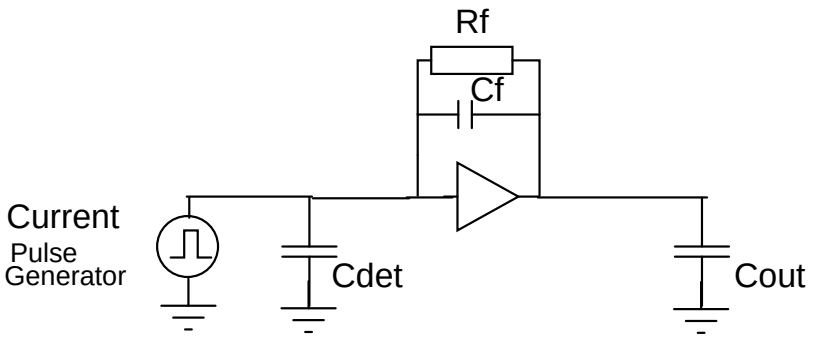

Figure 2.13: Simulation circuit. A current pulse is injected at the amplifier input to simulate charge injection.

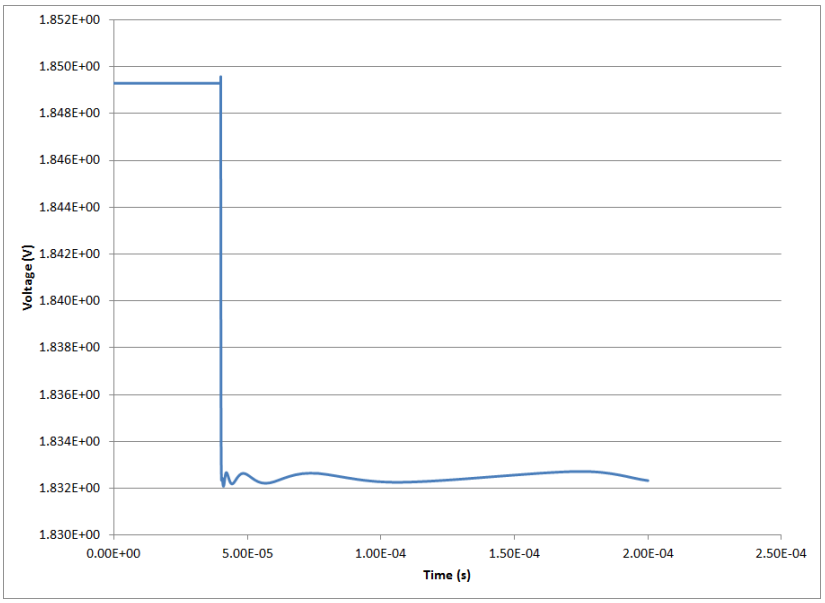

Figure 2.14: Simulated transient response to a current pulse equal to 24000 electrons.

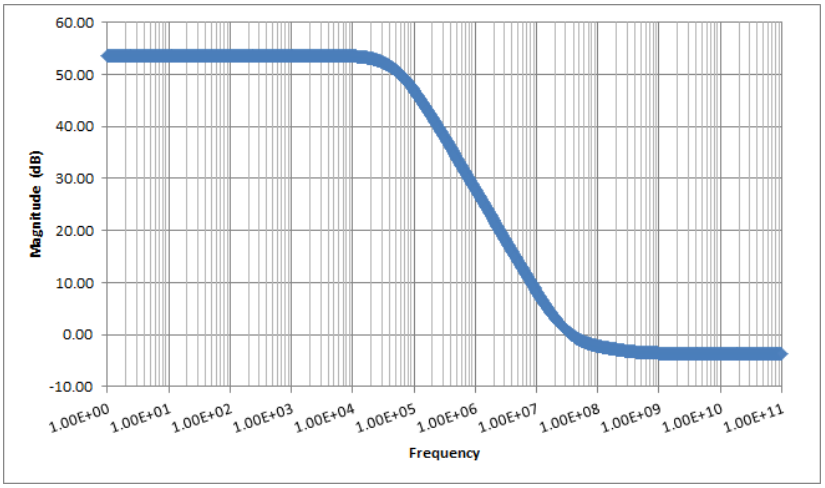

Figure 2.15: Simulated $Vout/I_{in}$ magnitude vs frequency response of CSA with load capacitance 0.1 pF.

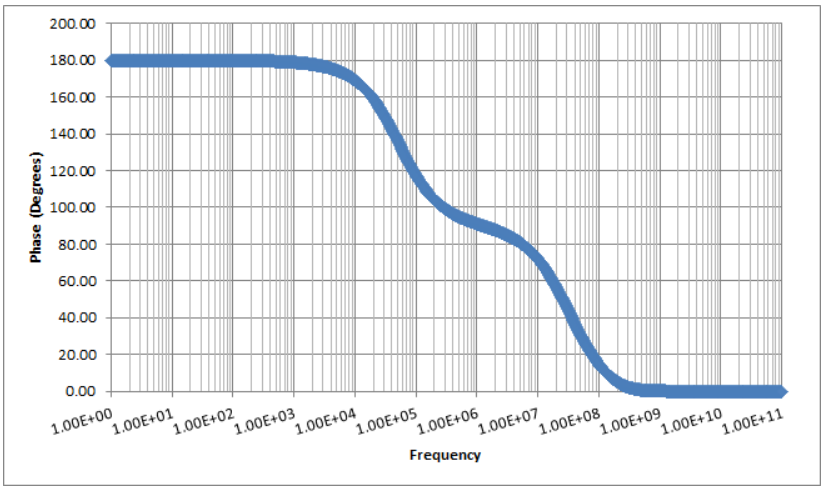

Figure 2.16: Simulated $Vout/I_{in}$ phase vs frequency response of CSA with load capacitance 0.1 pF.

2.4 CSA Layout

The CSA was fabricated in a 2 μm FD-SOI technology at WINFAB which provides one metal layer and one polysilicon layer to perform the circuit layout. The layout of the CSA is shown in Figure 2.17. Metal pads surround the layout to provide biasing with a probe station or for wire bonding. The feedback resistor is implemented with a long and thin nMOS transistor. The 0.2 pF feedback capacitor is made by overlapping an area of metal and polysilicon. Another capacitor of 1 pF is included between the power pad (Vdd=2.5V) and ground (VSS) to help maintain bias voltage stability. The area of the CSA layout, without bonding pads, is 300μm by 250μm.

2.5 DC Results

The first measurements performed on the amplifier were DC measurements. These measurements were performed with a probe station at the

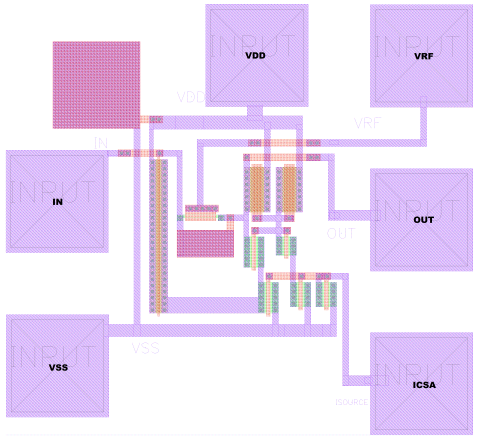

Figure 2.17: Layout of the CSA with metal bias pads labeled.

WELCOME facility in Louvain-la-Neuve. The amplifier was biased with a supply voltage of 2.5V and a bias current ICSA of 90μA. The input voltage was swept from 0V to 2.5V and the resulting output voltage was recorded to observe the amplifier's DC transfer curves. These curves were measured at different voltages applied to the back contact of the die. The measurements were performed in order to observe how the amplifier output differs from the nominal conditions when the substrate is biased.

The response to the back voltage is of particular interest as the eventual application for the amplifier is a monolithic detector, where the back plane will be biased to deplete the detector in the handle wafer. The handle wafer for this amplifier is p-type so if this amplifier were to be used as in a monolithic system, a negative voltage would be applied to the back contact. In this study, no detector was attached to the amplifier but measurements were performed to observe the behavior of the amplifier at different back voltages.

The results (the colored curves) are shown in Figure 2.18. The SPICE simulation corresponding to a back voltage of 0V, shown with black crosses, matches well with the measurement. The curve shifts as the back voltage increases, until about -3V when the output shifts out of

range. These first measurements demonstrate how biasing the back plane adversely affects the amplifier performance.

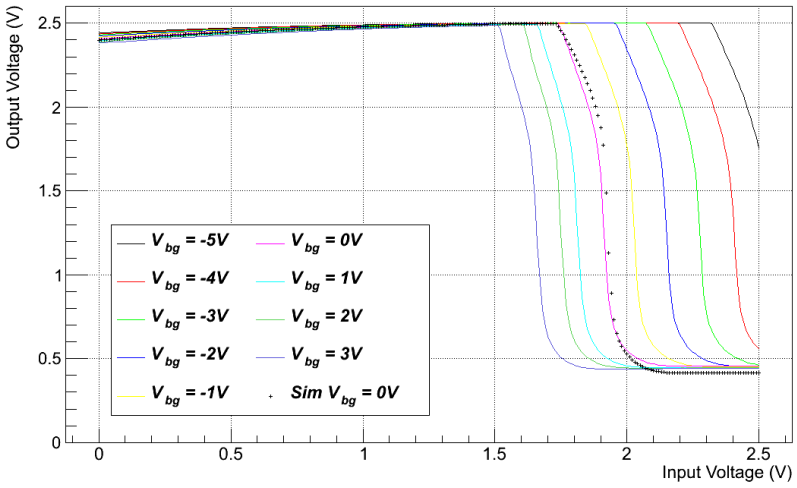

Figure 2.18: Measured DC curves at different applied back voltage.

2.6 Transient Results

The transient response of the amplifier was tested using a custom built test PCB (see Appendix A). The amplifier was bonded into a DIP package and an appropriate daughter board was created to accommodate the package as pictured in Figure 2.19. The test PCB contains DACs and amplifiers configured as current regulators to bias the amplifier. The voltage and current sources are controlled by an FPGA which interfaces to a PC.

The transient response of the amplifier was tested with a voltage pulse generator and input test capacitor as shown schematically in Figure 2.20. A voltage pulse placed onto a series test capacitor generates a charge at the amplifier input. The resulting output of the amplifier was observed

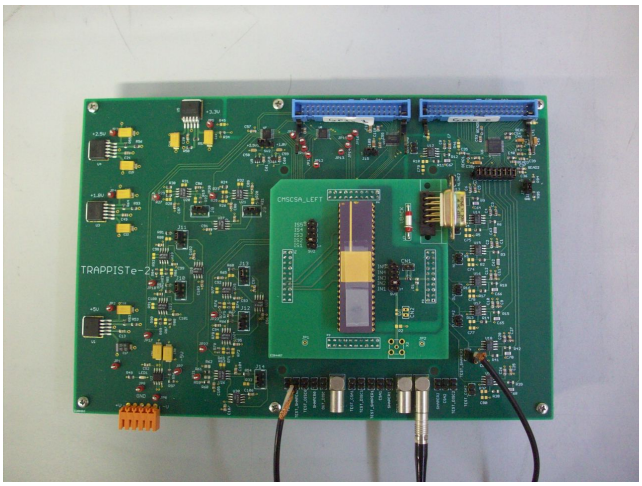

Figure 2.19: Daughter and main board for amplifier testing. Amplifiers are packaged in a DIP package.

and recorded on an oscilloscope, with results being averaged over 50 triggers. Measurements were taken with the oscilloscope AC coupled in order to observe the small voltage pulses.

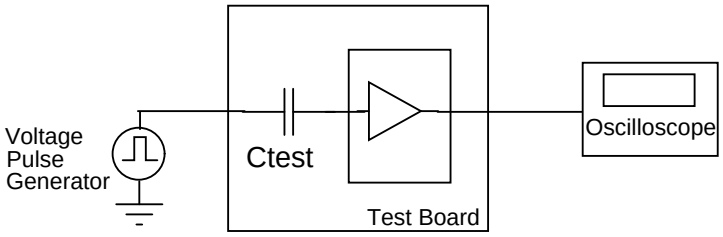

Figure 2.20: Transient test schematic. A voltage pulse is placed on a series test capacitor to inject a charge at the amplifier input.

The test capacitor with a value of 0.1pF was placed on the daughter board in series with the input to the amplifier. The voltage pulse placed on the capacitor had a risetime of 2.5ns to simulate the quick generation of charge generated by an incident particle. Table 2.2 gives the equivalent charge injected for different input voltages. MIPs are calcu-

lating assuming 24000 electrons per MIP, valid for a 300 μm thick silicon detector.

Voltage (V)	Coulombs	Electrons	MIPs
0.05	5.00E-15	3.13E+04	1.30
0.10	1.00E-14	6.25E+04	2.60
0.25	2.50E-14	1.56E+05	6.51
0.50	5.00E-14	3.13E+05	13.00
0.75	7.50E-14	4.69E+05	19.50
1.00	1.00E-13	6.25E+05	26.00
1.50	1.50E-13	9.38E+05	39.10
2.00	2.00E-13	1.25E+06	52.10
2.50	2.50E-13	1.56E+06	65.10

Table 2.2: Charge Input Calculation on 0.1pF Capacitor

The measured transient response of the CSA is shown in Figure 2.21 at different gate voltages on the feedback transistor V_{rf} . Measurements were taken with AC coupling on the oscilloscope in order to observe the small pulse signals. The amplifier was biased at the nominal VDD=2.5V and a bias current ICSA of 100 μA. A charge equivalent of about 100 000 electrons or 4.2 MIPs was injected at the input of the CSA. The expected gain of the amplifier is 18mV/MIP which should result in an output step voltage of about 75mV. The maximum measured step is just over 50mV, less than the expected value. This may be a result of the test setup, as the test capacitor is placed externally on the daughter board. Some of the charge generated at the test capacitor may be lost before it reaches the amplifier input inside the DIP package.

The effect of the feedback transistor can also be observed in Figure 2.21. A simulation of the amplifier shows how the pulse shape varies as the feedback resistance changes (Figure 2.22). The simulation was performed with a charge injection of 24000 electrons. As the feedback resistance value decreases, the time constant of the signal discharge $R_f C_f$ also decreases and the signal more rapidly reaches its nominal output value.

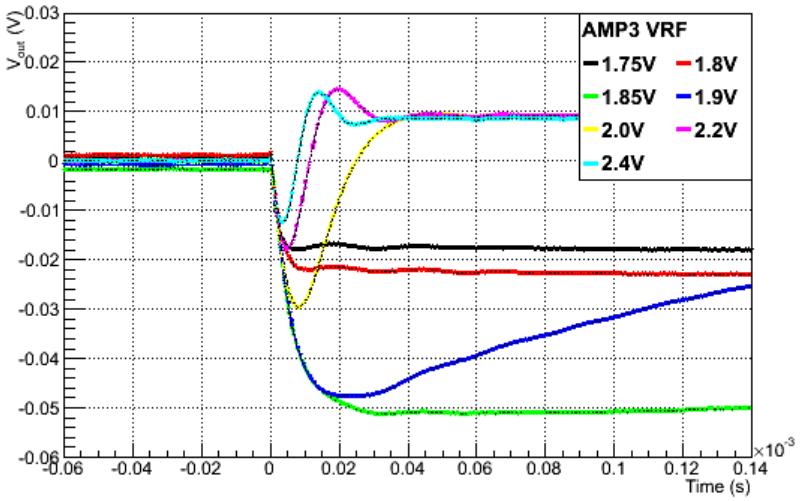

Figure 2.21: Measured CSA transient response (AC coupled) with sweep of feedback transistor voltage.

Table 2.3 shows the relationship between V_{rf} and the feedback resistance value. It shows the simulation results of the on resistance R_{ON} of the feedback transistor for the different V_{rf} values. A standalone nMOS transistor was simulated with the same dimensions as the feedback transistor (W/L = $3\mu m/30\ \mu m$). A small voltage of 5mV was placed across the drain and source and the gate voltage V_{rf} was varied. The source voltage was set to 1.8V to be representative of the amplifier bias conditions.

As V_{rf} is increased, R_{ON} decreases. A lower R_{ON} results in a lower feedback time constant $R_f C_f$ which results in a faster discharge of the output. From Figure 2.22, the step output response is maintained for resistance values above $10^{11}\Omega$. For lower resistance values, the output response begins to rapidly decay. From the simulated values, $10^{11}\Omega$ corresponds to approximately 1.9V on the gate of the feedback transistor. This value is close to the observed measurements shown in 2.21, where V_{rf} values up to around 1.85V provided step responses. Larger V_{rf} values result in decreased feedback resistance and a faster output discharge. Also from Equation 2.30, the resistance values are larger than

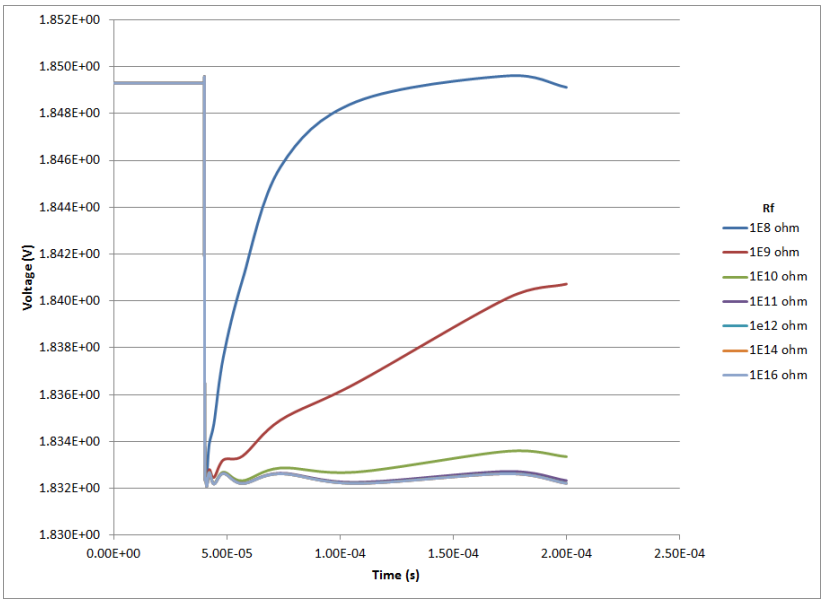

Figure 2.22: Simulated CSA transient response with sweep of feedback resistor values.

the assumed 100MΩ, which would decrease the first pole and result in a slower amplifier response.

Two parasitic effects should be considered when observing the measured transient results: leakage current and parasitic capacitance. The leakage current is particularly important when discussing charge amplifiers for detectors as the sensor connected to the CSA input will draw a constant leakage current. If this leakage current is drawn from the amplifier through the feedback resistance, the DC set point of the amplifier will be affected. Figure 2.23 illustrates the output when a 5pA leakage current is introduced. 5pA is representative of the leakage current in a pixel detector as discussed in Section 4.2. As the resistance values increase, the leakage current creates a larger voltage drop across the feedback resistance and the DC output set point can not be maintained. At 5pA and a feedback resistance of $10^{11}\Omega$, the DC output level drops to 1.35V. This can prove to be problematic if the leakage current is too high. For high

V_{rf}	R_{ON} (Ω)
0.5	8.7401E+17
1.0	3.5478E+17
1.3	8.9393E+15
1.4	1.8096E+15
1.5	3.2099E+14
1.6	5.0909E+13
1.7	7.3330E+12
1.8	9.7124E+11
1.9	1.1948E+11
2.0	1.3765E+10
2.2	1.5843E+08
2.5	1.8879E+06

Table 2.3: Simulated R_{ON} values for the feedback transistor

leakage currents or very high resistance values, the DC set point will be moved out of range. This will lead to a decrease in DC gain or if the level is shifted too much, the amplifier output pushed to its operational limits and be saturated. During testing of this amplifier study, the amplifier was not connected to any detector. However, any parasitic leakage current would create a shift in DC output level, even if very small. This would become more apparent at high resistance values or at low values of V_{rf}. At low V_{rf} values, the DC gain may be lower than nominal or if the DC output has shifted too low, the output may saturate. There may also be parasitic capacitances from the feedback transistor. This capacitance in parallel with the feedback resistance would reduce the $V = Q/C_f$ gain (Equation 2.26).

Another parasitic to consider is capacitance. A falltime of 100ns was previously simulated (Figure 2.14) however measured falltimes are closer to $10\mu s$. This is most likely the result of the measurement setup as the output of the CSA is routed off the test PCB to coax cables connected to an oscilloscope. This added parasitic load capacitance results in a longer falltime and reduced amplifier GBW. During testing, cables up to

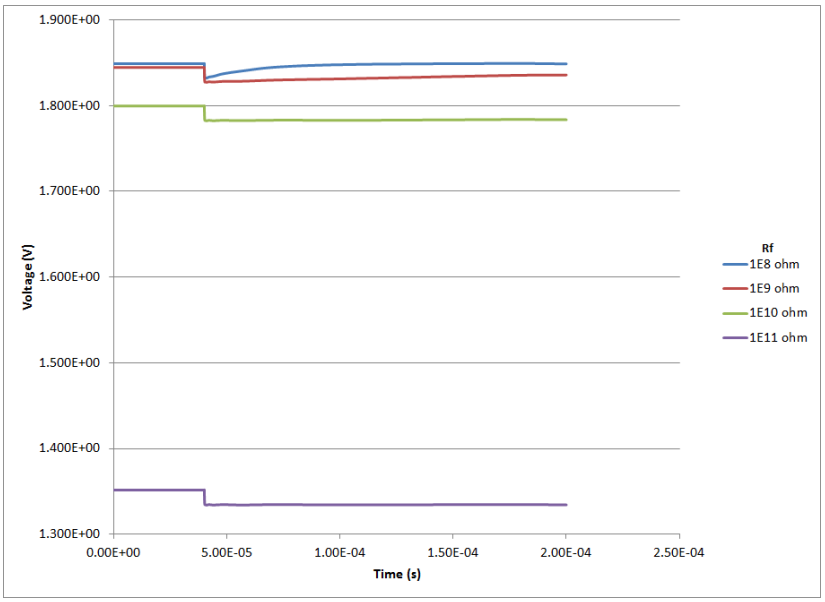

Figure 2.23: Simulated CSA transient response with sweep of feedback resistor values and 5pA leakage current.

2 meters long were used which could introduce as much as 200pF to the output of the circuit. In the simulated curves of Figure 2.24, a 200pF output load is added, resulting in comparable falltimes as the measured curves. The simulation was performed with a feedback transistor and a small parasitic leakage current of 0.1pA (SPICE required a small current to simulate properly). In the simulated curves, the DC component of the output has been removed to show how the measured curves vary. One can see that the falltimes of the signals has increased due to the parasitic load capacitance. As V_{rf} is increased the output discharges more quickly. For lower V_{rf} values, the height of the signal is reduced. This might be related to increased capacitances in the feedback transistor which would decrease the $V = Q/C_f$ gain. Also if the leakage current has decreased the DC output level too much, the signal may saturate.

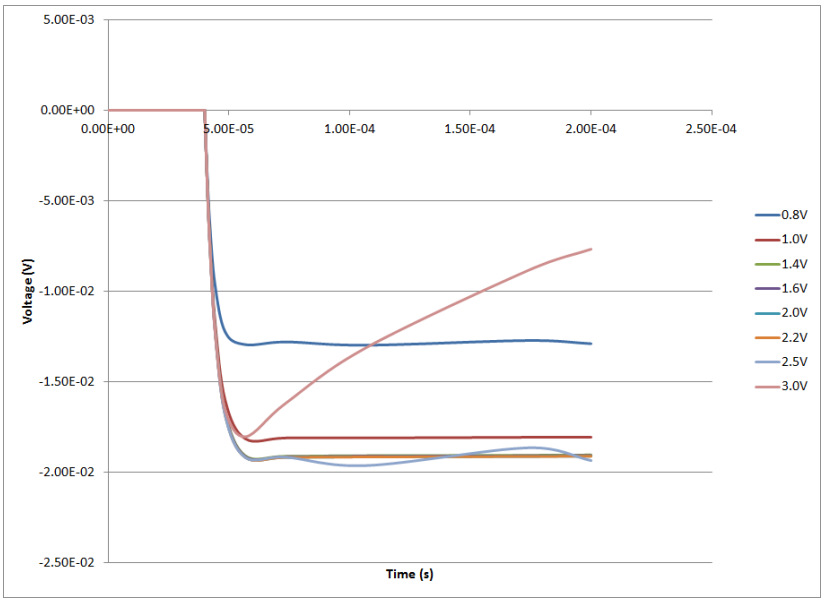

Figure 2.24: Simulated CSA transient response with sweep of feedback transistor voltage and 200pF output capacitance (DC component removed).

2.6.1 Transient Response to Back Voltage

The CSA is intended to be used in a monolithic detector system so the effect of applying a voltage on the metal back plane of the die is of particular interest. The transient output response to a charge injection of about 3 MIPs is shown in Figure 2.25 for a bias current of 100 μA and V_{rf} of 1.85V. The back voltage of the die is varied. For positive voltages, the risetime of the signal decreases as does the signal amplitude. As the handle wafer is a p-type substrate, the negative bias values would correspond to the depletion of a monolithic detector n-in-p sensor. For increased negative voltage, the signal amplitude is reduced. At a back bias of -1V, the amplification of the signal is already attenuated a factor of four from 40mV to 10mV peak voltage.

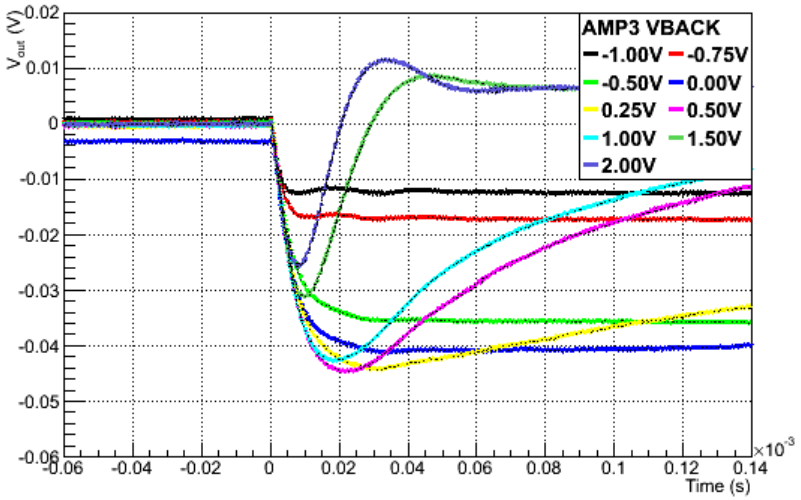

Figure 2.25: Amplifier transient response (AC coupled) to charge injection of around 3 MIPs with sweep of back voltage.

It was noted before that the amplifier response is quite sensitive to the feedback transistor voltage therefore any small change to the operation of the feedback transistor due to the back voltage would result in noticeable change in the transient response. The voltage applied to the back bias acts as an extra voltage applied to the gates of the transistors in the top layer. While the buried oxide layer provides some insulation between the readout circuit and sensor layers, this insulation is not perfect. While every transistor is being being affected by the back bias voltage, the circuit is particularly sensitive to the voltage on the feedback transistor. Therefore when a back bias is applied, the first observed effect is similar to the effect of varying the voltage on the feedback transistor.

To study effect, a simulation was performed in which the voltage at the substrate contact of the feedback transistor was varied. A small parasitic leakage current of 0.1pA was introduced to allow the SPICE simulation to operate properly. Figure 2.26 shows the result with the DC component removed. As back voltage is increased, V_{th} is effectively decreased and the feedback resistance decreases. The resulting output pulse decays quickly

as the $R_f C_f$ time constant is decreased. For negative back voltage, V_{th} is effectively increased and the feedback resistance is increased. With the presence of the leakage current, the DC output set point will decrease as the feedback resistance increases. The output will also saturate if shifted too far from its nominal DC level.

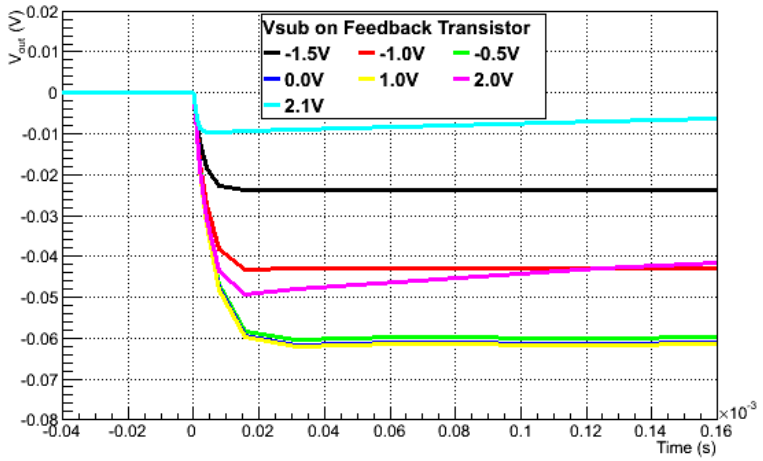

Figure 2.26: Simulated transient response with voltage applied to the substrate of the feedback transistor (DC level removed).

Figure 2.27 shows the measured amplitude response of the amplifier to increasing input charge at 0V and -0.75V back voltage. The first point of the graph is equivalent to an input charge of about 1.3 MIP (30000 electrons in 300 $/mum$ of silicon) with the last point at about 39 MIPS or 940,000 electrons. For a small applied back voltage, the amplitude of the charge curve is decreased by about one half. As a result, the amplifier as it is now would be difficult to implement in an monolithic system as its response varies strongly with the applied back voltage. It is possible to tune amplifier using V_{rf} to try to recover the DC set point when a back voltage is applied. However, this would be a limited solution and would not be able to cope with large applied voltages.

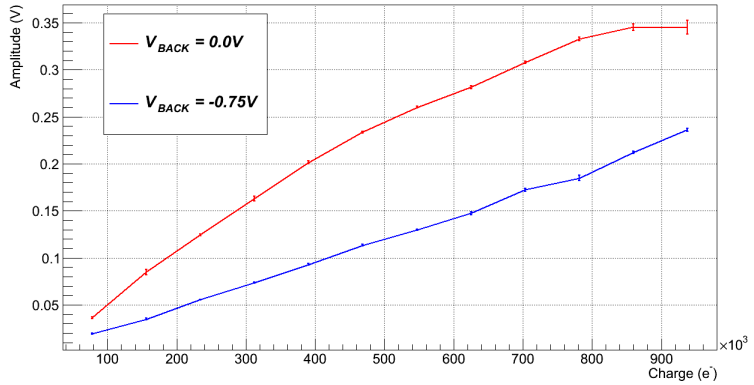

Figure 2.27: Measured amplifier charge curve amplitude response to back voltage.

2.7 Conclusion

A charge sensitive amplifier study has been realized in 2.0 μm FD-SOI CMOS technology and validated with measurements and SPICE simulations. Electrical testing showed that the amplifier is able to measure a charge injection down to around 30,000 electrons which is close to 1 MIP in 300 μm of silicon. Starting from detector and amplifier specifications, a top down synthesis of a CSA was developed. The amplifier is a standard operational transconductance amplifier with a folded cascode core. Collected charge is integrated onto a feedback capacitor and a feedback transistor is used to reset the charge signal. The amplifier was designed based on the detector specifications of CMS strip detectors. In particular, the capacitance of the strips was analyzed in order to calculate the noise performance of the amplifier. Based on the microstrip geometry, the capacitance was calculated to be on the order of 5pF and this value was used for the amplifier study.

Based on a g_m/I_D transistor sizing methodology, the transistors of the amplifier were then sized. First the input transistor, which directly interfaces with the detectors, was sized based on the calculated detector capacitance. The noise curve, plotted in Figure 2.8, showed that the

optimum input transistor size with respect to noise is around 1000 μm^2. A theoretical noise of 250 electrons is calculated, which is low enough to detect minimum ionizing particles in typical silicon detector widths on the order of 300 μm.

The other transistors followed by selecting g_m/I_D values and bias currents as illustrated in sizing schematic in Figure 2.12. The amplifier was then simulated in ELDO SPICE using the transistor models provided by the UCL facility and tuned to ensure correct functionality. One of them main advantages of the g_m/I_D methodology is its portability across technologies. The methodology relies on g_m/I_D curves which are extracted from process parameters. By keeping the same synthesis and substituting the g_m/I_D curves with those of the target process, the same methodology can be applied to the design of a CSA in another technological process.

The amplifier was fabricated at UCL's WINFAB facility 2 μm FD-SOI technology at WINFAB which provides one metal layer and one polysilicon layer. Initial DC tests were performed with a probe station directly on the wafer die. The amplifiers were biased at 2.5V and the DC voltage at the amplifier input was swept from 0V to 2.5V and the output voltage was recorded. The DC response of the circuit matched well with the expected simulation results as shown in Figure 2.18. The back plane of the wafer was biased to observe the behavior of the circuit under simulated detector biasing conditions. The wafer on which the amplifier was fabricated contains a P-type handle wafer. If a detector were to be implanted in the handle wafer, a negative voltage would have to be applied to the back plane to deplete the detector.

The transient response of the amplifier was then tested. The amplifier was bonded into a DIP package and mounted on a test PCB which provided the necessary biasing and input/output connections. Although no detector was attached to the amplifier, charge was injected via a series test capacitor placed at the amplifier input. The amplifier exhibited a proper transient response to test input charge as shown in Figure 2.21. During the test, it was possible to measure input charge signals of 1.3 MIP (Figure 2.27). With an improved measurement setup, the detection

of 1 MIP or less should be achievable which would be the minimum requirement for a particle tracking detector.

The effect of the feedback resistance was observed. As the voltage of the feedback transistor V_{rf} is increased, the feedback resistance decreases. This leads to a quicker discharge of the output signal as the time constant of the feedback is reduced. The effect of a leakage current was also observed. The presence of a leakage current results in a voltage drop across the feedback resistance which can disturb the DC bias point of the amplifier. As a result, the amplifier V_{rf} should be tuned depending on the leakage current conditions to set the correct amplifier DC bias point.

Although the general response of the amplifier was as predicted, the measured fall time of the signal was much larger than expected. This was due to the parasitic capacitances in the test setup. The input and output signals were taken off the board with coax cables which resulted in slower measured response times. The measurements may have been improved by optimizing the test setup (for example shortening cable lengths) or adding output buffers however this was not investigated further. Future developments could involve building a test board with an integrated on board readout system to obtain more accurate results.

The effect of the back gate voltage on the transient response is shown in Figure 2.25. The transient response of the amplifier to charge injection is very sensitive to the applied back bias. The back bias acts as an extra voltage applied to the gates of the transistors in the top layer. While every transistor is affected by the back bias, the circuit is particularly sensitive to the voltage on the feedback resistor. As a result, when the back bias is applied, the output first varies as if the voltage on the feedback resistor have been changed. With a charge injection of about 3 MIPs, the nominal signal voltage with no back voltage is 40mV. With an applied back voltage, the output amplitude decreases rapidly; at a bias voltage of -0.75V the output decreases to half its nominal value. At such low voltages, the depletion region in the handle wafer would be almost negligible making the detection of any incident particle difficult. The back voltage acts as an extra gate voltage on the top transistors. It was

observed that the amplifier is particularly sensitive to the voltage on the feedback transistor as this dictates the feedback resistance. While it is possible to tune V_{rf} to counter the back voltage, this approach will be limited in effect and would not be able to handle large back biases.

The main application of this amplifier is to work in a monolithic sensor. This first amplifier test was done without any detector implementation but it has it has been shown that the amplifier is able to detect input chargers on the order of a few MIPs. First measurements with an applied back bias show a degradation of amplifier performance. This back gate effect is a subject of study in the following chapters which describes the TRAPPISTe project's progress towards building a fully integrated detector.

CHAPTER 3

Overview of TRAPPISTe Devices

This chapter describes the first devices developed in the TRAPPISTe project. The first device, TRAPPISTe-1, was produced in 2009 and contained a small pixel matrix developed in UCL technology. This device was the project's first attempt to integrate a sensor with readout using SOI technology. It was fabricated at UCL's WINFAB facility in a $2\mu m$ FD-SOI CMOS process. This device consisted of an 8x8 pixel matrix with a 3T readout circuit integrated into each pixel. Due to processing errors, all transistors were subjected to a shift in threshold voltage and no meaningful measurements could be made.

Building on the experience gained from TRAPPISTe-1, a second device was developed in a more advanced technological process. TRAPPISTe-2 was designed in 2010 in a multi-project wafer run in $0.2\mu m$ FD-SOI OKI Semiconductor technology as part of the SOIPIX collaboration. The design consists of several test areas which include standalone test transistors and test amplifiers. These test structures were measured to characterize the process technology and amplifier performance. Two

pixel matrices are also present: one with a 3-transistor (3T) readout and another with an amplifier readout to investigate the performance of an integrated pixel detector in SOI technology.

3.1 TRAPPISTe-1

TRAPPISTe-1 was the first attempt in the TRAPPISTe project to develop a monolithic detector in SOI technology. The TRAPPISTe chip was fabricated at the WINFAB facility at UCL's Ecole Polytechnique de Louvain. This facility, inaugurated in December 2007, provides a teaching and research platform for students and researchers at the university.

The chip was fabricated in a 2μm Fully Depleted SOI CMOS process. The wafer consists of a p-type handle wafer substrate about 400-500 μm thick with a resistivity of 15-25 $\Omega \cdot cm$. To build a detector, higher resistivity substrates are more desirable as they allow for easier depletion of the sensor area. Figure 3.1 shows the depletion width of a $25\Omega \cdot cm$ substrate as a function of applied bias voltage. At 40V of bias voltage, the depletion depth is only 10μm of the up to 500μm thick substrate. However, this substrate was the only one available at the time of fabrication. The top wafer layers contain a 400 nm thick buried oxide layer and a 100 nm thick silicon active layer in which the device circuitry is implemented.

The UCL process provides four transistor types with different thresholds voltages V_t (nMOS/pMOS):

- Standard V_t (0.48V/-0.48V)
- High V_t (0.77V/-0.95V)
- Low V_t (0.24V/-0.08V)
- Graded channel

The graded channel transistors contains an asymmetrically doped channel that has been shown to give improved analog performance [85].

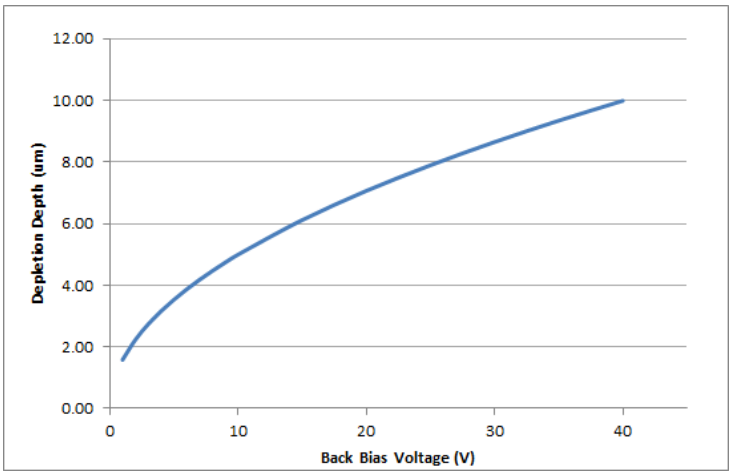

Figure 3.1: Depletion width versus bias voltage for a $25\Omega \cdot cm$ substrate

ELDO SPICE models were provided for the standard, high and low V_t transistors for simulation of the readout circuits however no SPICE models were available for the graded channel transistors.

3.1.1 TRAPPISTe-1 Overall Layout

The TRAPPISTe-1 chip is shown in Figure 3.2. The total size of the device is 3000 μm x 3000 μm. A series of bonding pads is implemented on the outer edge of the chip area. These pads are routed to the internal bias voltages and input/output signals in the matrix and are to be used to wire bond the die into a component package.

The overall layout of the TRAPPISTe-1 chip is shown in Figure 3.3. The center on the layout of the chip consists of an 8×8 matrix of pixels. A shift register implemented above the pixels controls the readout of the matrix. For each row of pixels, there is one associated output pad, for a total of 8 row outputs. The shift register activates one column at a time, connecting a pixel in each column to its associated row output pad.

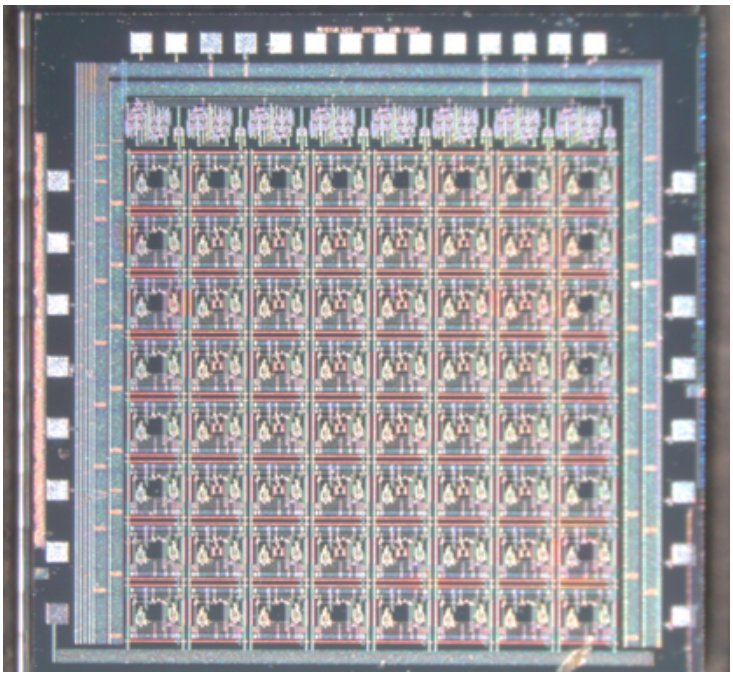

Figure 3.2: TRAPPISTe-1

The pixel matrix is divided into five areas named standard V_t, high$_t$, low$_t$, graded$_t$ and reset structures. These areas correspond to the type of transistor found in the pixel. Every pixel contains the same readout circuit composed of a different type of transistor. The standard V_t pixels contain standard V_t transistors, high V_t pixels are made up of high V_t transistors and so forth. In this way, the available transistor types could be tested to determine which one is best suited for pixel applications. The outermost pixels are called reset pixels. They differ from the inner pixels in that they do not contain any detector implant; they only contain the readout circuit realized with standard V_t transistors. These outer reset pixels can be used as test structures or they can be grounded to provide better isolation of the chip.

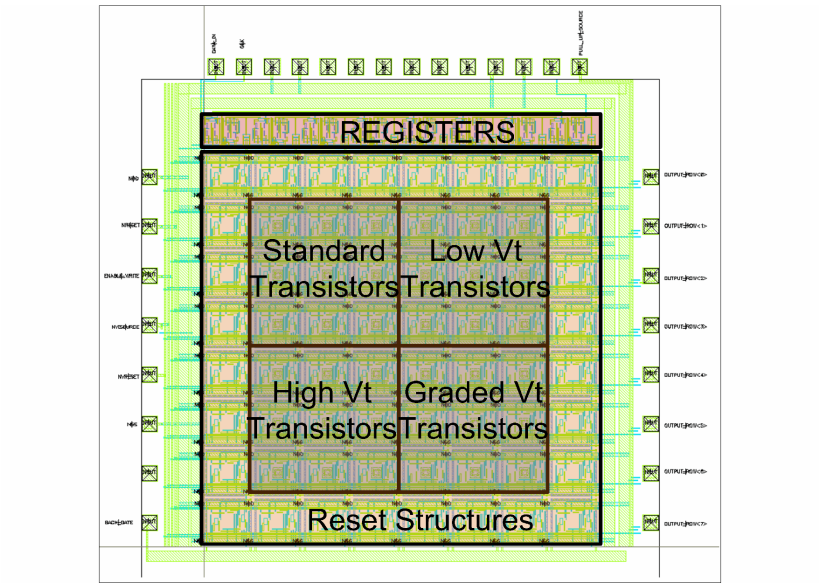

Figure 3.3: TRAPPISTe-1 overall layout with bonding pads on the outer edge and pixel matrix with shift register readout in the center.

3.1.2 Pixel Layout

In order to create a monolithic pixel sensor in SOI wafer, the technological process steps had to be planned out. First, a 60×60 μm^2 hole in the buried oxide is created. Through the hole, an n-type ($5{\cdot}10^{16}$ - $4{\cdot}10^{17}$ atoms/cm^3) implant is created in the bottom handle layer. This n-p junction, when biased, serves as the detector. To connect the detector to the readout electronics, a contact between the detector implant and a metal line is made. To reinforce the contact with the metal layer, an n++ doped area ($1{\cdot}10^{20}$ atoms/cm^3) is created in the detector implant area. A cross-section of a pixel detector contact is shown in Figure 3.4.

The detector implant is created in the center of the $300\mu m \times 300\mu m$ pixel. A total of four metal contacts to the detector implant are created per pixel to ensure good contact is made. The metal line is then routed out to the readout electronics. While placing the metal contact on the detector implant, care is taken not to cover the entire implant in metal.

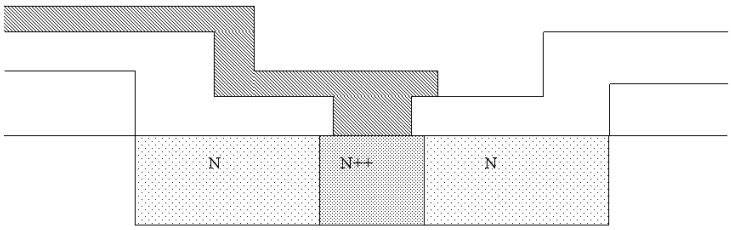

Figure 3.4: TRAPPISTe-1 pixel detector contact made with metal through a hole in the buried oxide layer.

Planned testing of the device involves illumination of the pixels from the topside with a laser for testing, therefore unobstructed access to the sensor area is required.

The readout circuit is implemented around the detector area. Due to the $2\mu m$ feature size of the technology, the majority of the pixel area is taken up by the readout transistors. Finally, a $10\mu m$ wide p+ guard ring is created around each pixel to provide insulation between pixels. The pixel layout is shown in Figure 3.5.

A description of the readout can be found in Appendix B. The readout is based on a 3-transistor topology inside each pixel with a shift register controlling the overall matrix readout. This first matrix was developed in parallel with the amplifier study so it was decided that a simpler 3-transistor readout would be used as the functioning of the amplifier was not yet verified. Also, the limited pixel area promoted the use of a minimum number of transistors.

3.1.3 TRAPPISTe-1 Production

The first TRAPPISTe-1 chip was produced in 2009. However due to process errors, all transistors exhibited a threshold voltage shift affecting the proper operation of the device. Despite the defect, the devices were bonded to test PCBs, shown in Figure 3.6. Electrical characterized was attempted with a custom built readout board but no meaningful

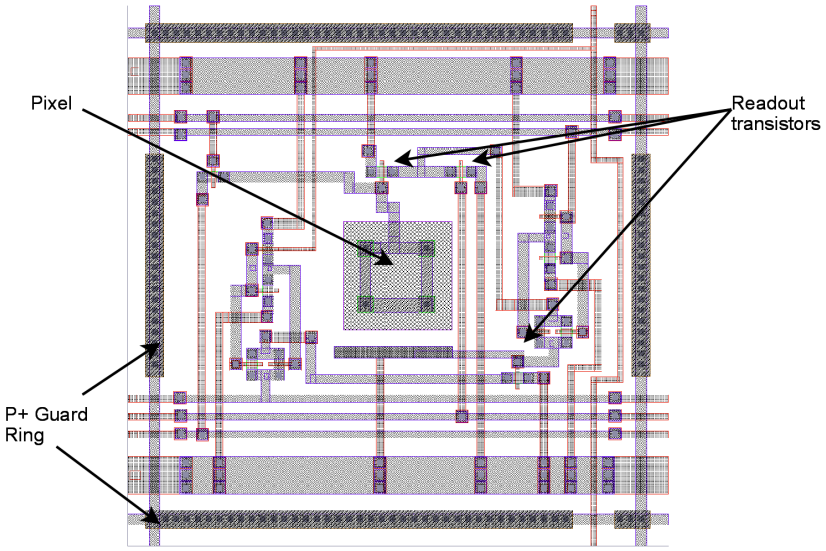

Figure 3.5: Layout of a TRAPPISTe-1 pixel cell. The sensor implant is made in the center of the pixel with the readout electronics surrounding it.

measurements could be extracted. Despite the fact that the first TRAPPISTe chip did not function, a lot of practical experience was gained regarding technological process, layout constraints and readout architecture. These lessons were directly applied to the second iteration of the TRAPPISTe chip, TRAPPISTe-2.

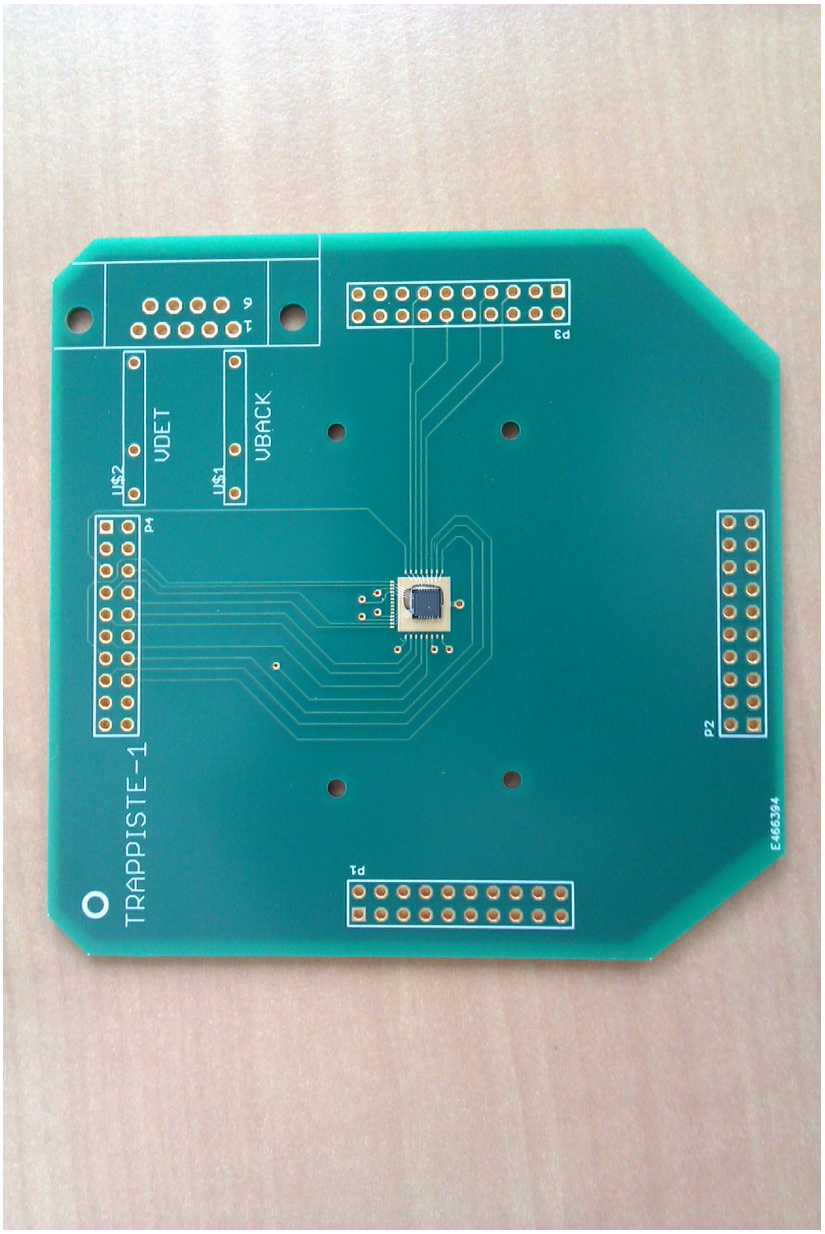

Figure 3.6: TRAPPISTe-1 bonded onto a PCB.

3.2 TRAPPISTe-2

TRAPPISTe-2 is the second in a series of chips designed to test the feasibility of building monolithic detectors in silicon-on-insulator technology.

Building upon the experience from TRAPPISTe-1, amplifier and matrix test structures were implemented in the layout. TRAPPISTe-2 is built with the OKI $0.2\mu m$ FD-SOI CMOS process. OKI Semiconductor was renamed LAPIS in 2011 however this thesis will refer to the OKI name used at the time of the fabrication of TRAPPISTe-2. TRAPPISTe-2 was part of a multi-project wafer (MPW) run within the SOIPIX collaboration. The SOIPIX collaboration is managed by KEK in Japan, which coordinates the activities within the collaboration.

The OKI process provides wafers with a $300\mu m$ n-type handle wafer, 200nm buried oxide and a 50nm active layer. Figure 3.7 shows a cross-section of the OKI wafer. To build the detector, p+ implants are processed in the n-type handle wafer and metal vias through the buried oxide provide contact to the implants. The detector diode may be depleted by applying a voltage to the back metal contact. An additional means of depleting the handle wafer is provided by a substrate contact (labeled Sub. Contact in Figure 3.7). Implemented as an n+ ring on the top side, the substrate contact permits the bias voltage to be applied to the top side of the handle wafer.

Compared to the UCL technology, the minimum feature size is ten times smaller: $0.2\mu m$ for the OKI process versus $2\mu m$ for the UCL process. The smaller feature size allows for the development of smaller pixels. The reduction in layout area of the readout circuits permits a larger percentage of the total pixel area to be devoted to collecting passing particles. The OKI process also provides 5 metal layers compared to UCL's 1 metal layer, which allows for denser and more intricate circuit layout.

Figure 3.7 also illustrates a new technology process made available by OKI: the buried p-well layer (BPW). The buried p-well is implanted below the buried oxide and can be placed underneath the transistors in the active layer. This layer may be biased via a top-side contact in order to shape the electric field in the handle wafer. It has been shown that setting this layer to 0V is useful in protecting the electronics in the top active layer from the backgate effect [75]. At the time of the development

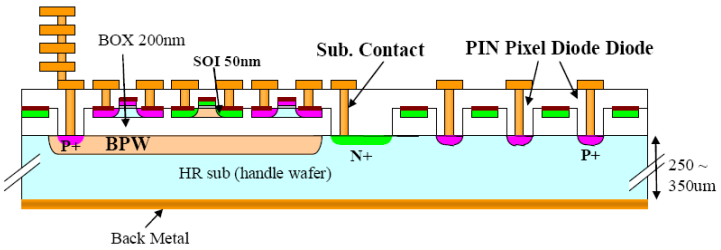

Figure 3.7: OKI wafer cross-section showing the implanted detector in the handle wafer and integrated electronics in the top layer.

of TRAPPISTe-2, the proper use of this buried p-well layer was not yet known. As a result, the buried p-well was not fully implemented in TRAPPISTe-2 but will be considered for use in the future TRAPPISTe-3, along with other advanced process techniques.

TRAPPISTe-2 was submitted in August 2010 as part of the MX1413 multi-project wafer run [86]. OKI provided libraries in Cadence Virtuoso for layout and SPICE models for simulation while KEK provided several layout macros for the development of pixel implants. The libraries included 5-metal layers and one polysilicon layer for circuit routing. Two types of source-tied transistors were available: standard threshold voltage (0.60V/-0.65V V_{th}) and low threshold voltage (0.37V/-0.33V V_{th}). The transistors are biased with a V_{ds} of 1.8V.

The SOIPIX collaboration had access to two high resistivity wafers: 700Ωcm and 10,000Ωcm. Compared to the UCL technology of $\approx$25Ωcm, the higher resistivity allows for a larger depletion zone with the same applied detector bias voltage. Figures 3.8 and 3.9 show the depletion width as a function of the applied bias voltage for 700Ωcm and 10,000Ωcm substrates respectively. In the UCL technology, an applied voltage of 40V resulted in only a 10μm depletion width as was shown in 3.1. With the availability of higher resistivity wafers from OKI, an applied voltage of 40V would give a 90μm depletion width for the 700Ωcm substrate and 340μm for the 10,000Ωcm substrate. The larger depletion width allows for a larger area for charge collection and therefore larger detec-

tor signals. The higher resistivity wafer also results in a lower detector capacitance, as was discussed in Section 2.1.

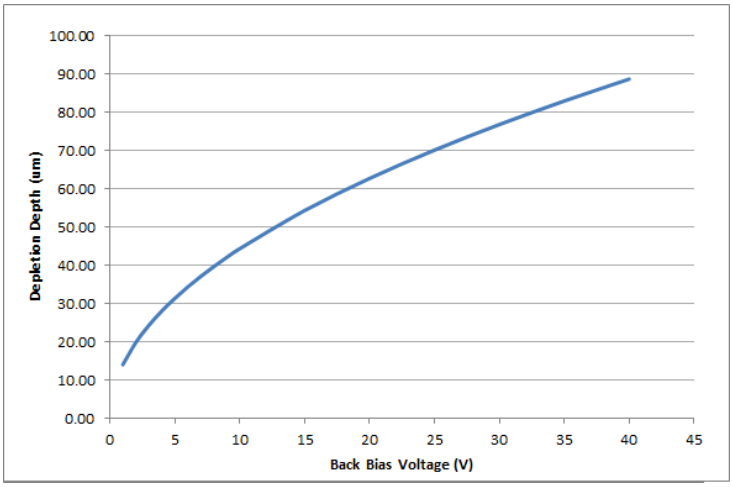

Figure 3.8: Depletion width versus bias voltage for a $700\Omega \cdot cm$ substrate

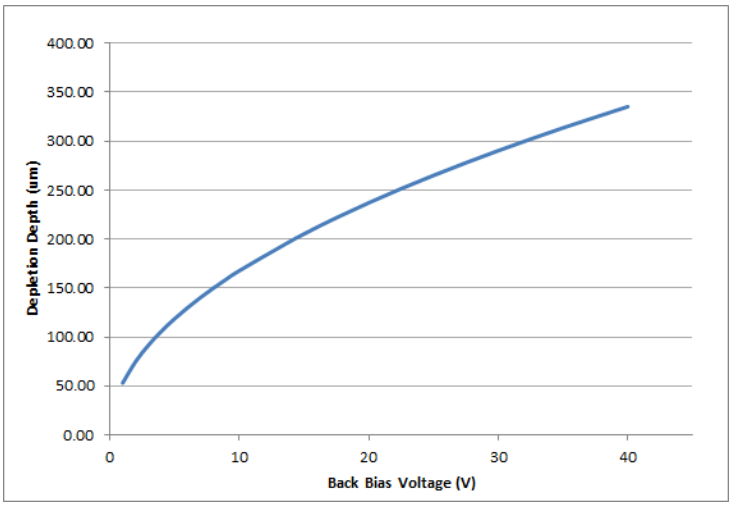

Figure 3.9: Depletion width versus bias voltage for a $10{,}000\Omega \cdot cm$ substrate

Several wafers of different handle wafer resistivity were processed and the following chips were provided to the TRAPPISTe project:

- 30 bare dies with a handle wafer of 700 Ωcm Czochralski silicon
- 10 chips in a PGA-256 package with a handle wafer of 700 Ωcm Czochralski silicon
- 10 chips in a PGA-256 package with a handle wafer of 10,000 Ωcm Float Zone silicon

The finished chips were delivered in January 2011. The packaged chips were bonded in PGA-256 packages at KEK. A photo showing a bonded TRAPPISTe-2 is shown in Figure 3.10.

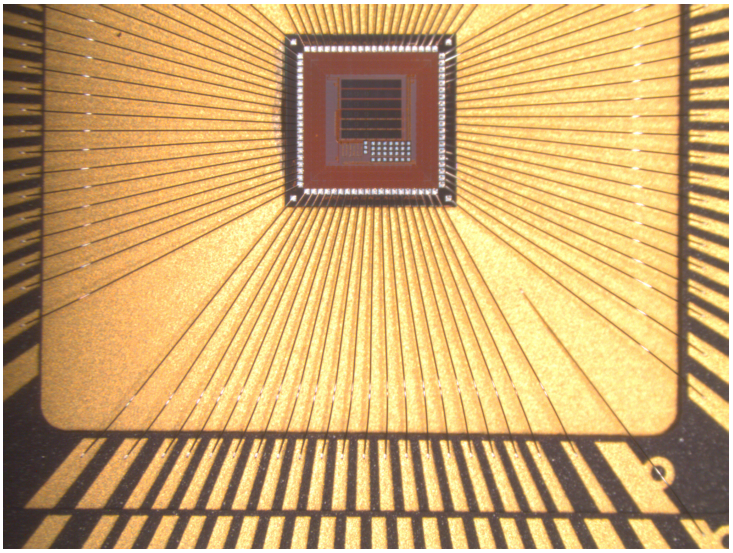

Figure 3.10: Bonding of TRAPPISTe-2 inside PGA-256 package.

In addition to the development of the TRAPPISTe-2 chip, the necessary testing environment was commissioned. A TRAPPISTe test PCB was built to provide the necessary biasing to the devices. The PCB is controlled by an FPGA which was programmed with the measurement test routines. More information on the TRAPPISTe PCB can be found in Appendix A.1. A laser system named LARA (Laser for Radiation Anal-

ysis) was also setup for stimulation with an infrared laser. The LARA system is described in Appendix A.2.

3.2.1 TRAPPISTe-2 Layout

The layout of the TRAPPISTe-2 chip is divided into several test areas. An outer input/output (IO) ring provided KEK surrounds the whole layout and the center contains standalone test structures and pixel matrices. The total outer dimensions of the TRAPPISTe-2 chip are 2.5mm×2.5mm. Figure 3.11 shows the overall layout of TRAPPISTe-2. The inner layout is divided into three main regions:

- The top region containing a 3-transistor (3T) matrix
- The middle region containing an amplifier matrix
- The bottom region containing transistor and amplifier test structures

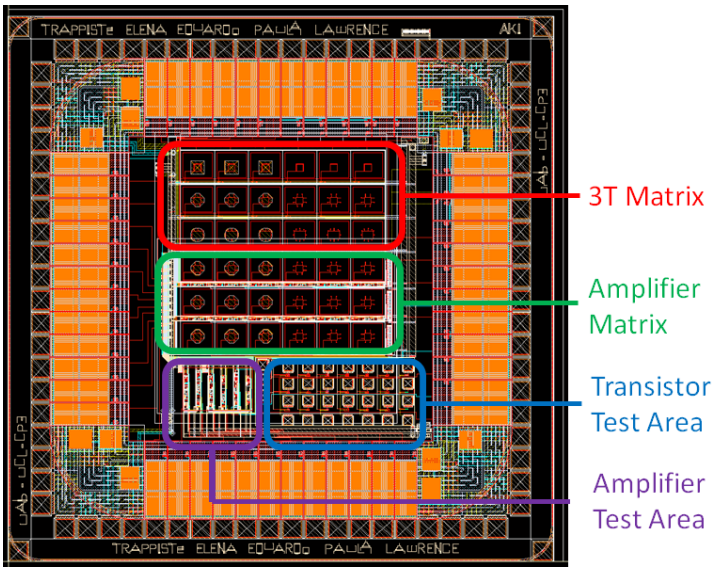

Figure 3.11: TRAPPISTe-2 overall layout

Input/Output Ring

The outer part of the layout consists of an IO ring whose layout was provided by KEK [87]. The IO ring provides bonding pads for wire bonding to a device package or PCB. These pads are placed in the ring as required by the layout designer and provide circuit buffering in addition to the metal bonding pad. Digital pads provide 3.3V low voltage TTL signals while the analog buffers provide protection diodes [88]. Signals are routed from the central circuits to the outer IO pads as required. The IO ring has space for 48 pads, 12 per side as shown in Figure 3.11.

In addition to bonding pads, the ring contains buffers and several bias and guard rings. Figure 3.12 shows a cross-section of the bias rings implemented in the IO ring. The P+ bias ring is used to bias the detector in the handle wafer. It is nominally grounded and a voltage applied to the back contact of the chip, V_{back}, is used to deplete the pixel sensor. The N+ substrate contact ring provides a direct contact to the handle wafer and may be used to deplete the detector area from the top side of the chip with voltage V_{det}.

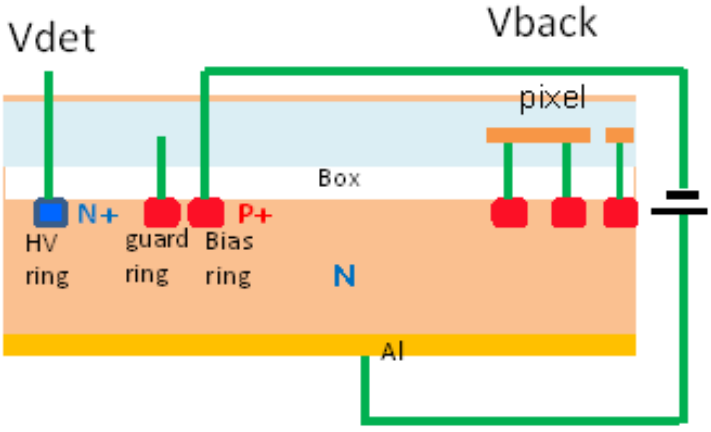

Figure 3.12: Bias Rings

In each of the four corners of the IO ring, bias pads are provided to access the different supply voltages and implanted rings. These pads are shown in Figure 3.13. The type of pads provided are:

- VDD33: 3.3V bias for the transistors in the IO ring.
- VDD18: 1.8V bias for the transistors in the central core area.
- VSS: Ground connection.
- VHV: Bias for the substrate contact N+ ring in the handle wafer (equivalent to V_{det} in Figure 3.12).
- VIO_BPW: Bias for a buried p-well implemented under the IO buffers to protect them from the backgate effect. Nominally connected to ground.

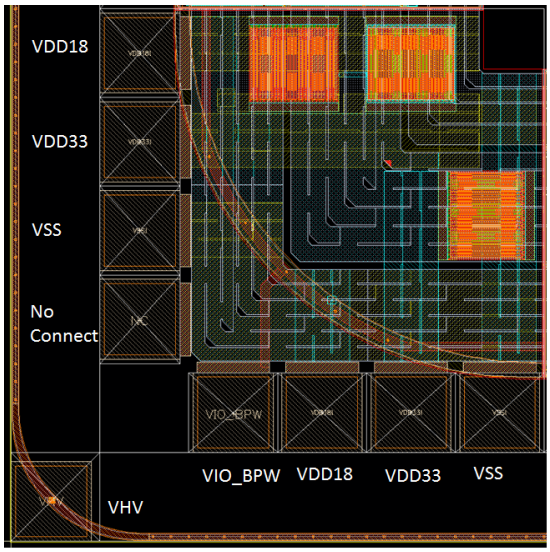

Figure 3.13: Corner pads of IO ring.

3.2.2 Transistor Test Area

TRAPPISTe-2 was the first experience in the TRAPPISTe project in using OKI technology. It was decided that a test area be implemented

to study the behavior of the OKI transistors. In particular, the effect of applying a back voltage to the substrate back contact is of interest in a monolithic pixel detector. The transistor test area contains individual transistors whose gate, source and drain inputs are connected to nearby test pads. These test pads are not connected to the outer IO ring and are meant to be tested with a probe station directly on the die.

The transistor test matrix contains 7 columns of transistors as shown in Figure 3.14. In each column, three of the same type of transistor are implemented. These transistors represent all the source tied transistors provided by the OKI process. They are divided into core and IO transistors. Core transistors are intended to be used in the inner circuits with a bias voltage of 1.8V. IO transistors are meant to be used in the IO ring and are biased at 3.3V. All of the transistors have a W/L of $10\mu m/2\mu m$ except for the I/O Depleted MOS (DMOS) transistors which are size $2\mu m/10\mu m$. Table 3.1 shows the complete list of test transistors.

Transistor	Type	Place	Voltage Threshold
T11, T12, T13	PMOS	IO	Standard Voltage
T21, T22, T23	PMOS	Core	Standard Voltage
T31, T32, T33	PMOS	Core	Low Voltage
T41, T42, T43	NMOS	IO	Standard Voltage
T51, T52, T53	NMOS	Core	Standard Voltage
T61, T62, T63	NMOS	Core	Low Voltage
T71, T72, T73	N-Type	IO	DMOS

Table 3.1: Type of transistors in the test area.

In each column, the gates of the three transistors are connected together and are accessed by the pads below each column, labeled G1-G7. There are three Source test pads labeled S1-S3. One source pad (S1) is connected to the DMOS transistor sources, the second (S2) is connected to the NMOS transistor sources and the third (S3) is connected to the PMOS transistor sources. The drains of all transistors each have their own individual test pad connection designated D11-D73.

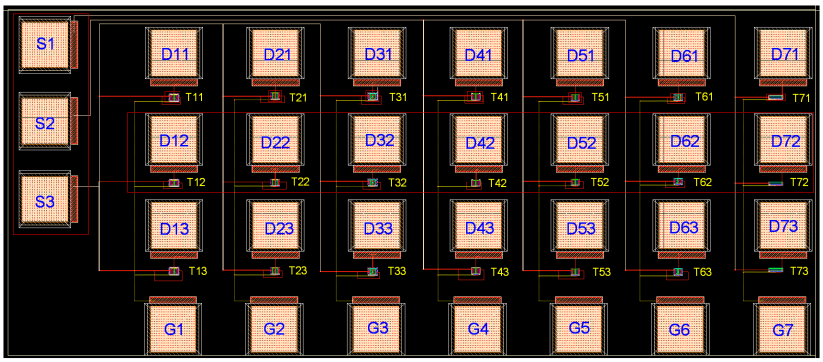

Figure 3.14: Layout of the transistor test area with transistors T11-T73, drain test pads D11-D73, gate test pads G1-G7 and source test pads S1-S3.

Figures 3.15 to 3.18 show the results of varying the back voltage on the test transistors. The drain voltages were set to 0.1V and the gate-to-source voltage was varied between 0V to 1.8V. Shown in the figures are the drain current vs gate-source voltage plots ($I_d - V_{gs}$)for the core transistors, both standard and low voltage. These four transistors are the type used in the development of the TRAPPISTe-2 readout circuits. The voltage at the bottom of the handle wafer is biased with a positive voltage, as would be the case in a monolithic detector where the n-type handle wafer is depleted.

While the pMOS remain relatively unaffected by the back voltage, there is a noticeable shift in the $I_d - V_{gs}$ curves for the nMOS transistors. As the positive back voltage increases, the threshold voltage of the transistors decreases. At 20V of back bias, the nMOS transistors are already turned on with a gate voltage V_{gs} of 0V. These results are in line with measurements taken by OKI, which show the susceptibility of the nMOS transistors to the back gate effect. [89].

The backgate effect has been a main subject of study for the SOIPIX collaboration and techniques such as the buried p-well [75] and nested wells [73] have been developed to mitigate the effect. These techniques

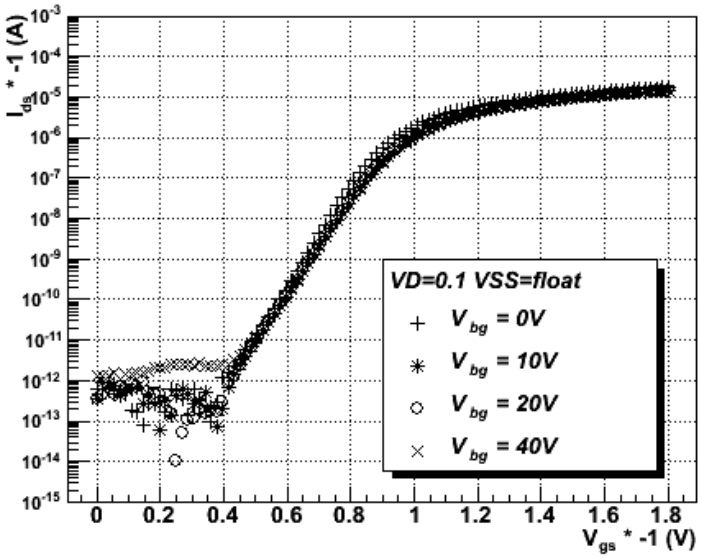

Figure 3.15: PMOS standard voltage $I_d - V_{gs}$ curves with varying back voltage

were not fully realized in TRAPPISTe-2 but are planned to be used in the future TRAPPISTe-3.

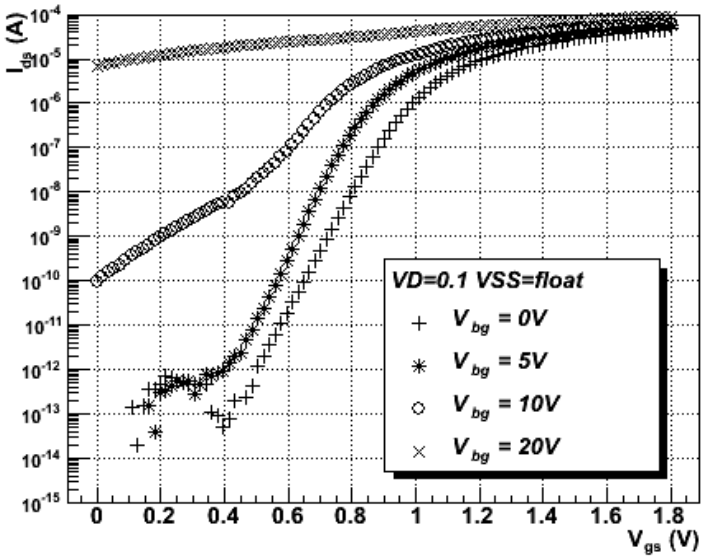

Figure 3.16: NMOS standard voltage $I_d - V_{gs}$ curves with varying back voltage

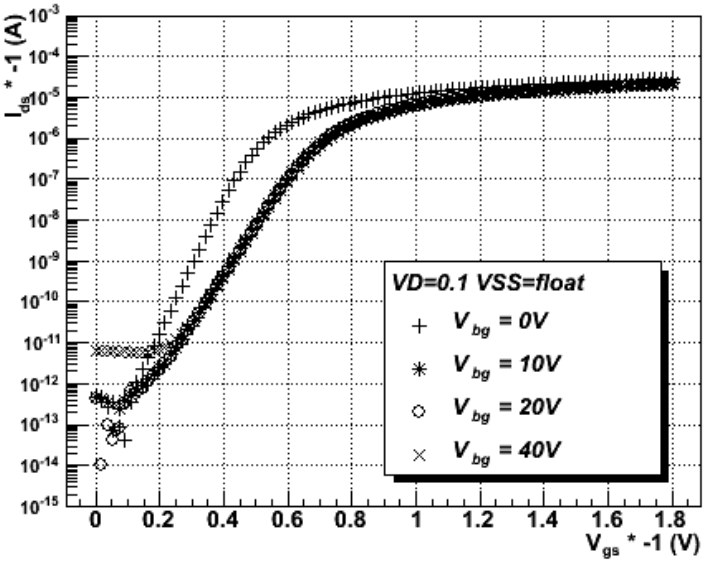

Figure 3.17: PMOS low voltage $I_d - V_{gs}$ curves with varying back voltage

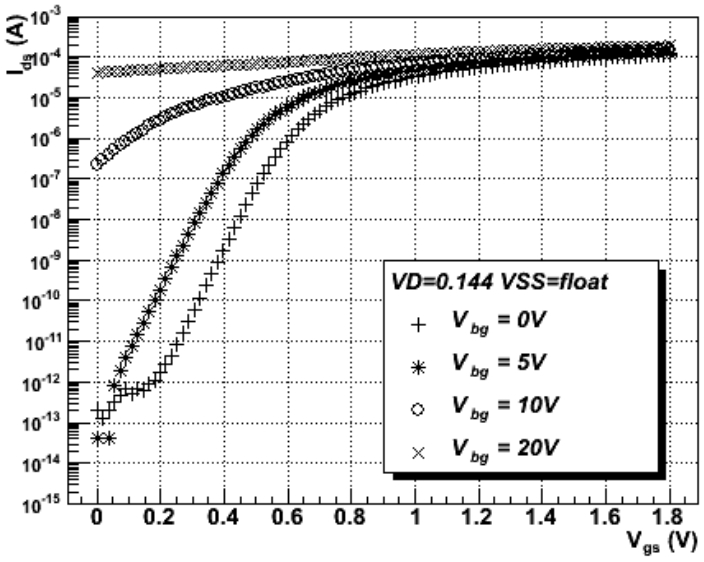

Figure 3.18: NMOS low voltage $I_d - V_{gs}$ curves with varying back voltage

3.2.3 3T Matrix

Building upon the experience gained from TRAPPISTe-1, a pixel matrix with integrated 3-transistor readout was implemented in the TRAPPISTe-2 chip. The new pixel matrix used the same readout architecture as the previous matrix however with the more advanced OKI technology (OKI $0.2\mu m$ FD-SOI CMOS vs. UCL $2\mu m$ FD-SOI CMOS), smaller pixels could be realized. The pixel matrix was placed in the top region of the TRAPPISTe-2 layout (Figure 3.11).

The 3T matrix is a 6 column by 3 row pixel matrix as shown in Figure 3.19. Each pixel is $150\mu m \times 150\mu m$ and contains the pixel implant in the center of the pixel with a 3-transistor readout chain placed below. In comparison to TRAPPISTe-1 which had $300\mu m \times 300\mu m$ pixels, the pixel size area has been reduced and a larger proportion of the pixel (about 90 percent) is free of circuitry, allowing for more efficient detection of incident particles.

Each row of the matrix contains an implant with a different shape. The top row contains a simple square implant, the middle row an octagonal implant and the last a rounded implant. It has been shown by other research groups in the SOIPIX collaboration that the shape of the implant influences the breakdown voltage of the detector [90]. Unfortunately no direct access to the pixel implant was foreseen on TRAPPISTe-2 so this could not be verified.

The 3T readout on TRAPPISTe-2 is described in Appendix B. It is similar to the readout architecture implemented on TRAPPISTe-1.

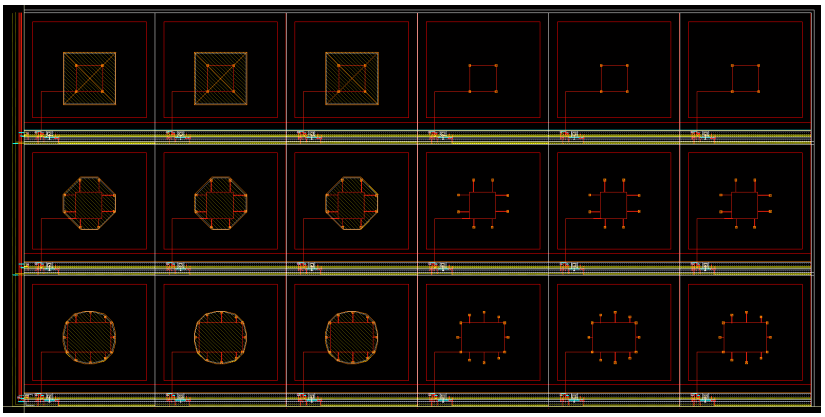

Figure 3.19: Layout of the 3T matrix. Each row contains a different implant shape.

3.2.4 Amplifier Test Area

The $0.2\mu m$ OKI process, compared to the $2\mu m$ UCL technology, allows for a denser circuit layout. The smaller feature size coupled with the increased number of metal interconnect layers (4 metal layers with OKI vs. 1 with UCL) permit more complex circuitry to be placed in the same area. It was decided to incorporate a more advanced readout circuit than the 3T readout in TRAPPISTe-2 to make use of the advanced technology.

A charge sensitive amplifier and shaper were implemented using the same methodology developed in the UCL charge amplifier study (see Chapter 2). The design and test of the amplifiers are described in Chapter 4; this section will only the describe the layout of the amplifiers and test structures.

As this was the TRAPPISTe project's first experience with OKI technology, a set of amplifier test structures were implemented. The test amplifiers contained a charge sensitive amplifier connected to a shaping amplifier. These structures are not connected to any detector implant and are only intended for electrical characterization testing. The inputs, outputs and bias signals of these test amplifiers are connected to the outer I/O ring surrounding the chip.

There are three different versions of the amplifier chain designated version 0, version 1 and version 2. These variants differ in the type of transistors used to create them and the amount of biasing required. The three circuit variants are:

- CSA0 and SHAPER0: Circuit with direct biasing composed of standard voltage transistors
- CSA1 and SHAPER1: Circuit with direct biasing composed of low voltage transistors
- CSA2 and SHAPER2: Circuit with biasing transistors composed of low voltage transistors

Version 2 of the amplifier uses the same architecture as the charge amplifier study in Chapter 2. It contains biasing transistors (Figure 3.21) which reduces the number of required control lines.

Version 0 and version 1 of the amplifier contain amplifier structures which require direct biasing as shown in Figure 3.20. These two versions of the amplifier were implemented in case the self-biasing version did not function correctly. Direct biasing provides more control of the amplifier and it was hoped that a working set of biases could be found if the self-biasing version 2 of the amplifier did not behave properly. Version 0 was made with standard voltage transistors and version 1 with low voltage transistors to further increase the chances of finding a working circuit. The drawback to providing direct control of the amplifier is that more signal lines are required which may be problematic as this increases the complexity of the circuit layout in an already dense pixel matrix.

As described in Chapter 4, version 2 of the amplifier did function correctly and testing was performed principally on this version. Version 0 and version 1 also worked and their results can be found in Appendix C.

Figure 3.22 shows the layout of the amplifier test structures. The layout consists of six columns with each column containing either stand-alone amplifier structures or an amplifier chain containing a CSA and shaper connected together. The amplifier chains also contain a 37.5fF input

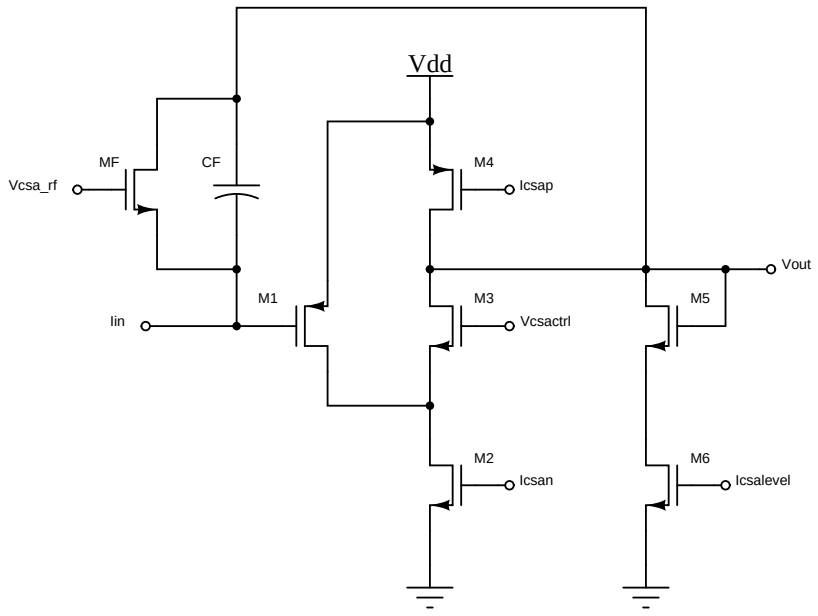

Figure 3.20: Amplifier with direct biasing (CSA0 and CSA1)

series capacitor which can be used to inject charge at the entrance of the CSA. Table 3.2 lists the structures in the layout.

Column	Contents	Notes
1	Amplifier Chain V0	Series input 37.5fF capacitor
2	CSA V0, Shaper V0, Discriminator	-
3	Amplifier Chain V1	Series input 37.5fF capacitor
4	CSA V1, Shaper V1	-
5	Amplifier Chain V2	Series input 37.5fF capacitor
6	CSA V2, Shaper V2	-

Table 3.2: Test structures containing either stand-alone amplifiers or an amplifier chain containing a CSA and shaper connected together. Layout shown in Figure 3.22.

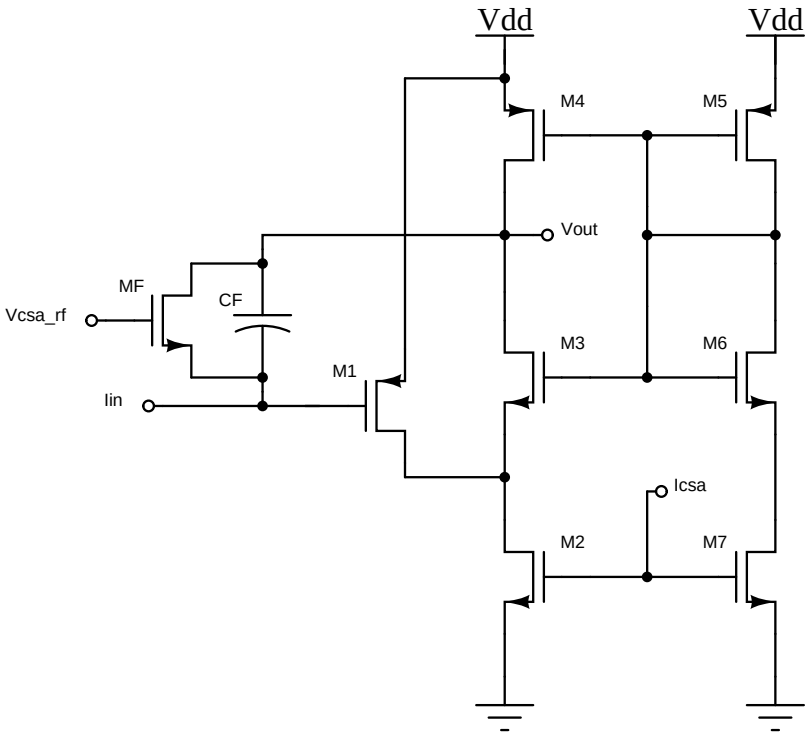

Figure 3.21: Amplifier with biasing transistors (CSA2)

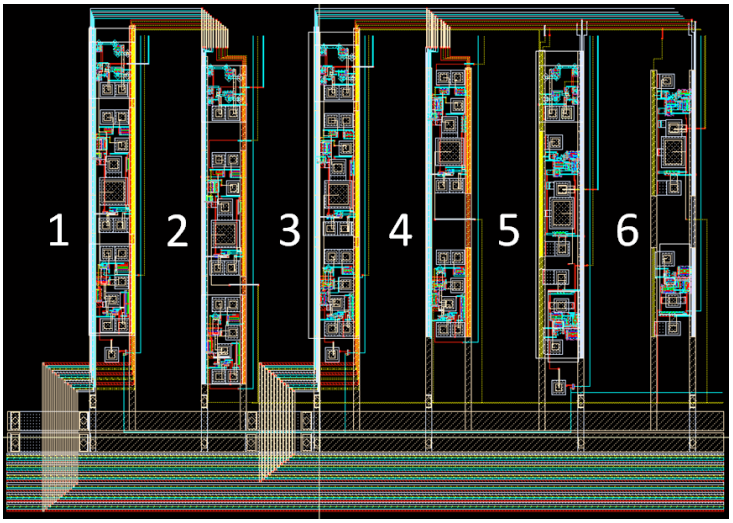

Figure 3.22: Layout of the amplifier test area.

3.2.5 Amplifier Matrix

The middle region of the layout contains the complete monolithic pixel detector: a pixel matrix with integrated amplifier chain. The same amplifier chains as those in the amplifier test area are integrated into a 6 column by 3 row matrix of pixels. The readout chains contain a charge sensitive amplifier and a shaper. Each pixel is $150\mu m$ x $150\mu m$ with a pixel implant made in the center and the readout chain placed at the bottom of the pixel.

Each row contains a different version of the amplifier chain. The top row contains amplifier chain version 0, the middle row contains amplifier chain version 1 and the bottom row contains amplifier chain version 2 (Figure 3.23). As described in the Amplifier Test Area, versions 0 and 1 of the amplifier were created in case version 2 did not function correctly. As version 2 did work, testing of the amplifier matrix was performed mainly on the third row. The details and test results of the amplifier matrix tests are discussed in Chapter 5; this section only describes the layout of the matrix.

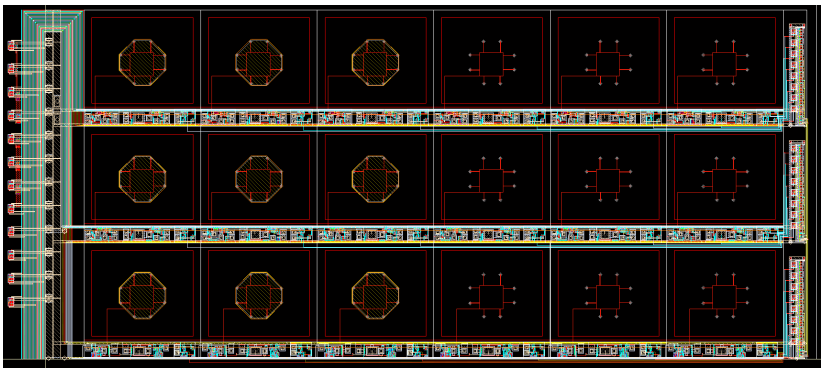

Figure 3.23: Layout of the amplifier matrix. The readout chain is placed in the bottom part of each pixel and a multiplexer is present at the end of each row on the right-hand side.

Due to the limited number of output pads on the IO ring, each row in the matrix is designated one output pad. In order to readout each of

the six pixels in one row, an 8-to-1 multiplexer is implemented (visible on the right side of the matrix layout in Figure 3.23). For the first five columns, only the output of the shaper in each pixel is connected to the multiplexer. In the last column, the outputs of the CSA, the shaper and a discriminator are connected to the multiplexer. The multiplexer output is controlled by three select lines which determine which pixel is connected to the output pad (Figure 3.24).

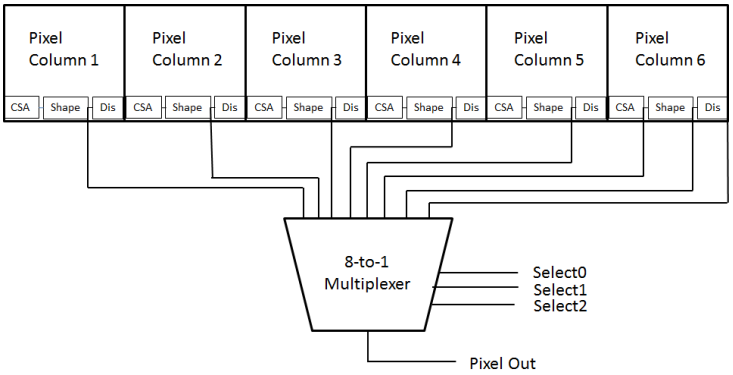

Figure 3.24: The amplifier matrix readout is controlled by an 8-to-1 multiplexer. One multiplexer is present on each row. Three select lines chose which pixel is placed on the output pad.

3.3 Conclusion

The TRAPPISTe project began in 2009 with the development of a first pixel matrix called TRAPPISTe-1. TRAPPISTe-1 was the first attempt at UCL to build a monolithic pixel detector in SOI technology. The device consisted of an 8×8 matrix with an integrated 3-transistor readout. It was developed in a $2\mu m$ FD-SOI CMOS process at UCL's WINFAB facility. Unfortunately, the first tape-out of the chip suffered from process errors which resulted in shifted transistor threshold voltages. While this first device did not function as intended, TRAPPISTe-1 provided a

first introduction to the tools and techniques required in developing a monolithic detector in SOI technology.

A second device, TRAPPISTe-2 was developed as part of a multi project wafer run as part of the SOIPIX collaboration. The SOIPIX collaboration provides access to OKI Semiconductor technology. For TRAPPISTe-2, a $0.2\mu m$ FD-SOI CMOS process was used. The smaller feature size, along with an increased number of metal lines, allowed for the implementation of smaller pixels with more advanced circuit integration.

The design of TRAPPISTe-2 followed directly from the experience gained during development of the TRAPPISTe-1 chip and CSA amplifier study. The g_m/I_D methodology was used to develop amplifiers in OKI technology and a small 3-transistor based pixel matrix was created with the same readout scheme as TRAPPISTe-1. As this technology was new to the TRAPPISTe project, a set of test transistors was also implemented. These standalone transistors were characterized and showed that the transistor threshold voltages are affected by an applied voltage bias on the backplane. At a back voltage of 20V, the nMOS transistors are open even with a gate voltage of 0V.

Several amplifier test structures were included in the TRAPPISTe-2 layout. These amplifiers were designed with the same methodology used in the CSA study described in Chapter 2. Several versions of the amplifier were created. Version 2 of the amplifier is self-biased and while version 0 and version 1 were directly biased. The directly biased versions were created as failsafes in case version 2 did not function. Version 2 did function in the end and was thus the main focus of testing. The discussion of its design and testing is the subject of the Chapter 4. Test results of the version 0 and version 1 can be found in Appendix C.

The culmination of the test structures and test matrices is a pixel matrix with an integrated amplifier readout. TRAPPISTe-2 contains a 3×6 pixel matrix with an integrated multiplexer to select pixel outputs. Each pixel is $150\mu m$ x $150\mu m$ and holds a charge sensitive amplifier and shaper amplifier. The size of these pixels compares favorably with current state of the art hybrid detectors used at the LHC. The CMS detector harbors detectors of size 150 μm × 100 μm and the ATLAS detector has typ-

ical pixel sizes of 50 μm $\times$ 400 μm. The successful physical layout of a monolithic pixel detector with integrated readout in a representative pixel size was an important milestone in the development of the TRAPPISTe detector. The matrix was tested with a laser source to test the collection of charge within the handle layer. The results of the amplifier matrix testing is detailed in Chapter 5.

CHAPTER 4

TRAPPISTe-2 Amplifiers

This chapter describes the test results of the amplifier test structures placed on the TRAPPISTe-2 chip. The TRAPPISTe-2 chip was developed as a proof of concept to characterize an amplifier chain in a monolithic SOI detector. As this was the TRAPPISTe's project first experience with the OKI $0.2\mu m$ FD-SOI process, a set of standalone test amplifiers were included to verify their electrical performance. These test structures do not have a detector implant at their input and are intended to be tested with standard current and voltage sources. The amplifiers implemented used standard amplifier architectures, based on the methodology developed during the amplifier study, and were implemented to observe their behavior under biasing detector biasing conditions.

The main goal of the testing was to qualify the transistor transient response to an input charge stimulus. The amplifiers are designed to be integrated into a monolithic pixel. As a result, their response to charge injection on the order of a minimum ionizing particle is important as

this is the amount of charge a passing high energy particle would deposit. Also, in a monolithic detector, a voltage is applied to the back metal plane to deplete the detector in the handle wafer, so the amplifier response to the backgate voltage is important.

The design of the test amplifiers followed from the methodology developed for the charge sensitive amplifier study done in UCL technology (see Chapter 2). One advantage of the g_m/I_D methodology is that the g_m/I_D parameter can be abstracted from the target technological process. While the design methodology was developed using UCL technology, it can be applied to the OKI process by keeping the same design flow and substituting in the g_m/I_D curves for the target OKI process. As the design flow had already been developed once for the CSA study, the initial design for the new TRAPPISTe-2 amplifiers was more quickly and easily realized.

The TRAPPISTe-2 amplifier design began with the development of a charge sensitive amplifier. The CSA is based on the same folded cascode architecture used in the charge sensitive amplifier study. The amplifier is intended to be integrated within a monolithic pixel so the detector specifications of a pixel sensor were used as the input detector. As the more advanced 0.2 μm OKI process with 5 metal layers allows for denser circuit layout than the 2 μm UCL process, it was decided to add a basic shaper amplifier at the output of the CSA.

Figure 4.1 illustrates the typical detector readout chain comprising a CSA and a shaper. The CSA converts the charge collected in the detector into a voltage output. The output of the CSA is a step-like voltage signal whose amplitude is proportional to the charge input. A typical shaper amplifier transforms the step-like CSA output into a semi-gaussian output signal. The semi-gaussian output signal is more easily processed by subsequent pulse processing electronics such as discriminators and ADCs. The shaper behaves like a bandpass filter consisting of a differentiator followed by one or more integrating stages. The TRAPPISTe-2 shapers contain an input series capacitor and resistor acting as a differentiator and one amplifier configured as an integrator.

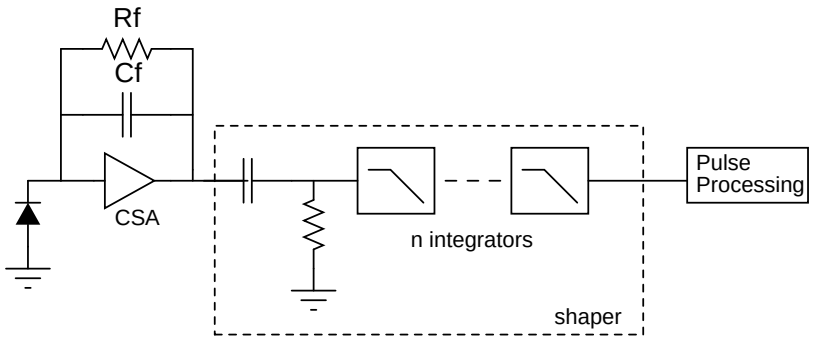

Figure 4.1: A typical detector read out chain showing the CSA and shaper consisting of an differentiator and several integrating stages. The TRAPPISTe-2 readout chain contains one integrating stage.

4.1 TRAPPISTe-2 Amplifiers

The TRAPPISTe-2 chip contains three varieties of charge sensitive amplifiers and shaping amplifiers. Charge sensitive amplifiers are referred to as CSA and shaping amplifiers are referred to as SHAPER. These amplifiers differ in the type of transistors used to build them and the type of biasing required to operate them.

- CSA0 and SHAPER0: Circuit with direct biasing composed of standard voltage transistors
- CSA1 and SHAPER1: Circuit with direct biasing composed of low voltage transistors
- CSA2 and SHAPER2: Circuit with biasing transistors composed of low voltage transistors

The transistors used in this design were source-tied core transistors provided by the OKI process [91]. The standard voltage transistors have nMOS/pMOS threshold voltages of 0.60V/-0.65V and the low voltage transistors have threshold voltages of 0.37V/-0.33V. SPICE models were provided by KEK for circuit simulation [92].

Version CSA2 of the TRAPPISTe-2 amplifiers uses the same architecture as that of the CSA fabricated in the charge amplifier study in Chapter 2. The same design methodology was followed with the parameters of the OKI technology substituted in where applicable. The versions CSA1 and CSA0 of the amplifier consist of just the cascode core of the amplifier with direct biasing of the core transistors. These directly biased versions were included on the chip as this was the project's first experience with OKI technology. The extra biasing signals provide more control over the amplifiers in case the self-biasing amplifiers did not function properly, at the expense of an increased number of control lines.

The $0.2\mu m$ OKI technology allows for denser circuit layout than the TRAPPISTe-1 technology so it was decided to also implement basic shaper amplifiers. As this device was a proof of concept a simple shaper was implemented. The shaper amplifiers were based on a design by Jan Schipper [93]. The shapers consist of an input series capacitor acting as a differentiator and an integrating amplifier to produce a semi-gaussian output signal. The core of the shaper is based on the same architecture as the CSA but with modified transistor sizes.

4.2 TRAPPISTe-2 Charge Sensitive Amplifiers

The TRAPPISTe-2 charge sensitive amplifiers use the same core architecture as the amplifiers in the TRAPPISTe-1 amplifier study. While the core of the all the amplifiers is the same folded cascode architecture, two different bias schemes were implemented: self-biasing transistors and direct biasing. The self-biased amplifier contains biasing transistor which provide bias currents and voltages based on the applied supply voltage. The directly biased amplifiers require voltages and source currents to be directly applied to the circuit.

Version CSA2 of the amplifier is built with the same architecture used in the charge amplifier study in Chapter 2. The cascode core comprised of transistors M1 and M3 is biased by several bias transistors as shown in Figure 4.2. An input current is integrated onto feedback capacitor CF

and a long transistor MF operating in the linear region acts as a resistive feedback. This amplifier was composed of source-tied low voltage transistors.

A second version of the CSA with direct biasing, shown in Figure 4.3, was also implemented. Bias voltages and currents are directly applied to the amplifier cascode core, while a small transistor M5 biased by M6 is set to regulate the DC output [93]. This version of the amplifier offers more control of the circuit and was implemented in case the self-biasing version did not work. Direct biasing versions of the amplifier were implemented using standard voltage (CSA0) and low voltage transistors (CSA1).

In case of failure of version CSA2, operating points could be individually set directly on the cascode core with versions CSA0 and CSA1. Direct biasing provides greater circuit control, however it requires more signal lines compared to implementing self-biasing transistors. This may pose layout problems in an already dense pixel matrix. Additional biasing lines also require more voltage and current sources, adding complexity to the supply electronics.

Upon testing of the amplifiers, amplifier version CSA2 did function correctly. As a result, CSA2 was the main focus of testing. CSA0 and CSA1 also functioned correctly and were tested less extensively. Those results can be found in Appendix C.

4.2.1 TRAPPISTe-2 CSA Sizing

The CSA was designed using the same g_m/I_D method employed previously in the charge amplifier study (see Chapter 2). Parameters based on the technological process and circuit performance were used as inputs into the design methodology to size the transistors. Since all the parameters of the OKI technology were not fully known at the time of design, estimates for the detector parameters were used. One extra criterion in the TRAPPISTe-2 amplifier design was to minimize the layout area of the amplifier. The amplifiers would eventually be incorporated into a

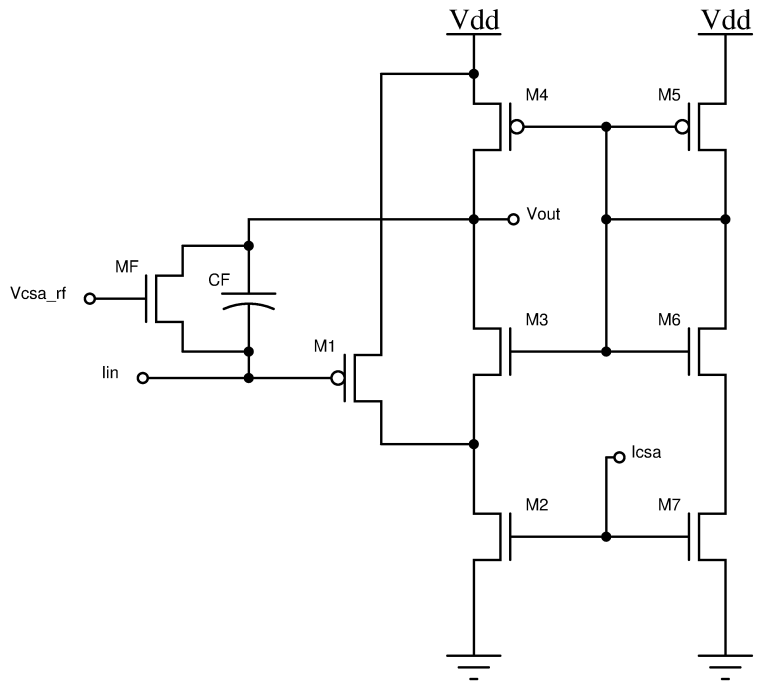

Figure 4.2: Amplifier with biasing transistors (CSA2)

monolithic pixel therefore a smaller layout area allows them to fit inside the pixel area and also permits the creation of smaller pixels.

The amplifiers were designed with an initial estimate of 10fF for the pixel detector capacitance which were calculated in Chapter 2. The feedback capacitor value is 37.5fF and was determined by the desire to have a compact layout area. With these initial values, a noise curve as a function of input transistor size for the TRAPPISTe-2 amplifier was calculated following the same noise equations as in Chapter 2. The curve was calculated for values of the flicker noise $K_f = 5 \times 10^{-31}\ C^2/cm^2$ and oxide capacitance $C_{ox} = 7.67 \times 10^{-15}\ F/\mu m^2$. An order n=1 shaper was assumed with a shaper shaping time of $1\mu s$.

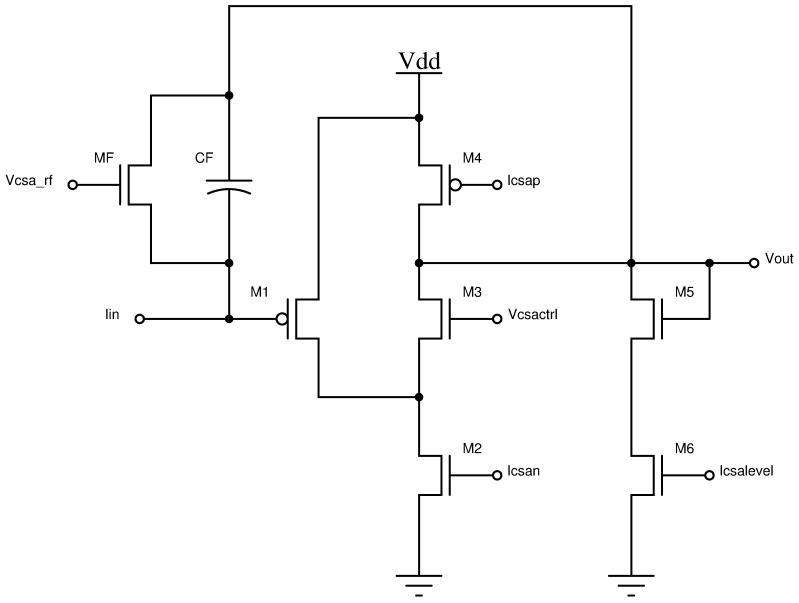

Figure 4.3: Amplifier with direct biasing (CSA1 and CSA0)

The leakage current of the pixel detector was not known but for an absolute worst case scenario, a leakage current of 500pA, the same as for the CMS microstrip detectors, was plotted (Figure 4.4). One can see that the high leakage current dominates the noise calculation. A more realistic leakage current may be obtained by considering the fact that the area of the pixel is about 100 times less than the area of the microstrip. One could therefore expect that the leakage current will be on the order of 100 times less than that of the microstrip. A plot of the noise curve with a leakage current of 5pA is shown in Figure 4.5 resulting in a low theoretical minimum noise of less than 10 electrons. While this level of noise seems extremely low, the MIMOSA series of detectors using a 3-transistor readout in epitaxial technology has demonstrated noise levels down to 14 electrons with a power consumption of about $250\mu W$ per pixel [94]. For both the 500pA and 5pA cases, the minimum of the noise curve is found at a transistor size of around 5 μm^2 so this size was used.

From these noise calculations, one can see how moving to a smaller feature size technology can improve pixel performance. The smaller feature size of the OKI process versus the WINFAB process allows for the creation of smaller pixels since the layout area of the circuit is reduced. Having smaller pixels means smaller sensor capacitance and lower leakage current, resulting in lower overall noise. The noise calculations for these pixels show that the noise is dominated by the leakage current and will therefore be dependent on the material properties of the sensor silicon.

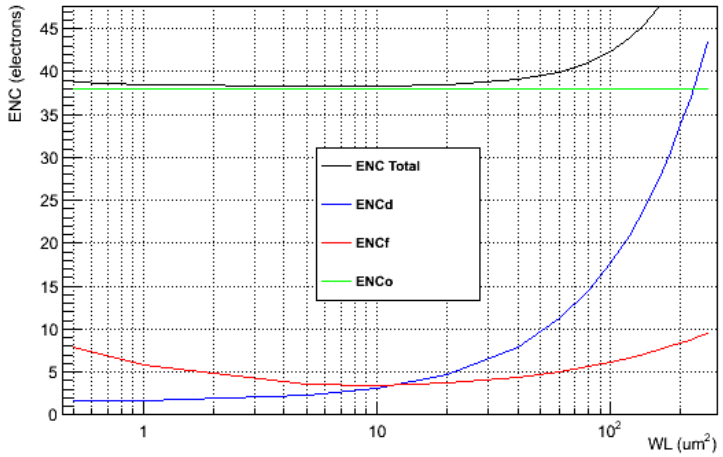

Figure 4.4: ENC Curve for TRAPPISTe-2 Amplifier with 500pA leakage current

Following the same transistor dimensioning methodology as for the amplifier study described in Section 2.3, the transistor dimensions of the TRAPPISTe-2 were chosen. The g_m/I_D curves used in the sizing methodology were generated from the OKI provided transistor models. Figure 4.6 shows the g_m/I_D characteristic curve for a low threshold voltage OKI transistor. A plot of the g_m/I_D curve for the UCL process is also shown for comparison. One can see that the more advanced OKI technology

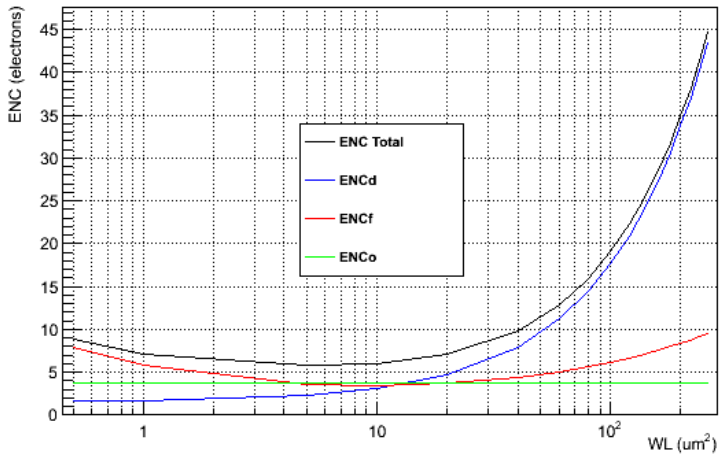

Figure 4.5: ENC Curve for TRAPPISTe-2 Amplifier with 5pA leakage current

is more efficient than the UCL technology, as it can achieve the same g_m/I_D amplification at lower currents.

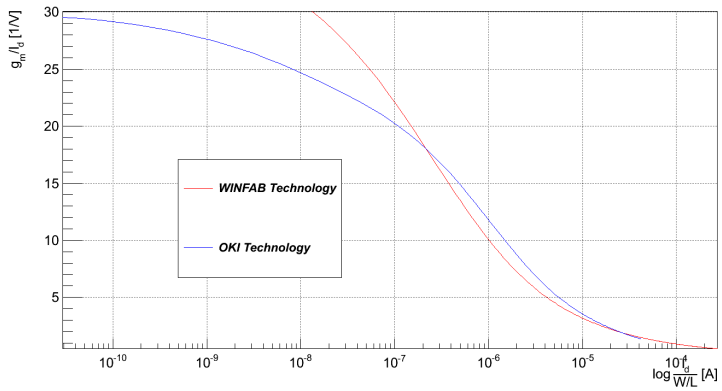

Figure 4.6: g_m/I_D curves for OKI and UCL WINFAB technology processes

As in the amplifier study, the outcome of the g_m/I_D methodology was simulated in ELDO SPICE and then modified as necessary to ensure proper operation. An effort was made to use the smallest size transistor sizes possible in order to integrate the amplifier into a pixel matrix. As a result, the smallest transistor length was often selected.

At the time of development, a decision was made to keep the amplifier bias current at $100\mu A$, the same as with the amplifier study. This was done to reduce the number of design variables and also served a practical purpose, in that the same readout board used in the amplifier study could be reused to test the TRAPPISTe amplifiers. It is expected that the power consumption for in the OKI process could be lowered in future designs, however for this proof-of-concept a $100\mu A$ bias current was maintained. Both the OKI and UCL technology amplifiers consumed about 400 μW of power. The final transistor sizes are shown in Table 4.1.

		W/L [$\mu m/\mu m$]		
Transistor	g_m/I_D	CSA2	CSA1	CSA0
M1	2.6	5/1	5/1	5/1
M2	4.3	4/0.5	4/0.5	5/0.8
M3	11.6	3/0.2	3/0.2	3/0.2
M4	13.3	10/0.2	10/0.2	5/0.2
M5	13.3	10/0.2	0.63/0.6	0.63/0.6
M6	4.8	0.7/0.2	1/0.6	1/0.6
M7	4.3	1/0.5	-	-
MF	-	0.7/10	0.7/10	0.7/10

Table 4.1: TRAPPISTe-2 CSA Transistor Dimensions

The layout of the amplifier is shown in 3.2.4. The layout area of the amplifier is about 50 μm by 40 μm. Compared to the larger UCL technology which had an amplifier area of $300\mu m$ by $250\mu m$, this is a 40 times reduction in area. A smaller layout area allows for the creation of smaller pixels and smaller pixels means a lower sensor capacitance. A lower sensor capacitance results in lower noise figures which is always

desirable. In terms of developing a pixel matrix, the OKI technology is more suitable. Also, the extra metal layers in the OKI technology allow for more complex circuit layout which may be required in a large pixel matrix. The UCL technology can still used for larger pad and strip detectors, however for pixels the OKI technology has a clear advantage.

A simulation of the transient output of the amplifier is plotted in Figure 4.7. To simulate charge injection at the input of the amplifier, a short transient current source is introduced at the detector diode as described in Section 2.3.3. An input current pulse of length 2.5ns and amplitude $1.55\mu A$ is applied to simulate a charge injection of around 24000 electrons, equivalent the charge deposited by a minimum ionizing particle in $300\mu m$ of silicon. The amplifier bias points are shown in Figure 4.2 and the bias current ICSA is 100 μA, the same as in the charge amplifier study. As with the amplifier study, the feedback resistance is simulated with a large resistor, this time with resistance $10^{12}\Omega$. The simulation shows an output amplitude of 85mV which is consistent with the feedback capacitance value of 37.5fF (V=Q/C).

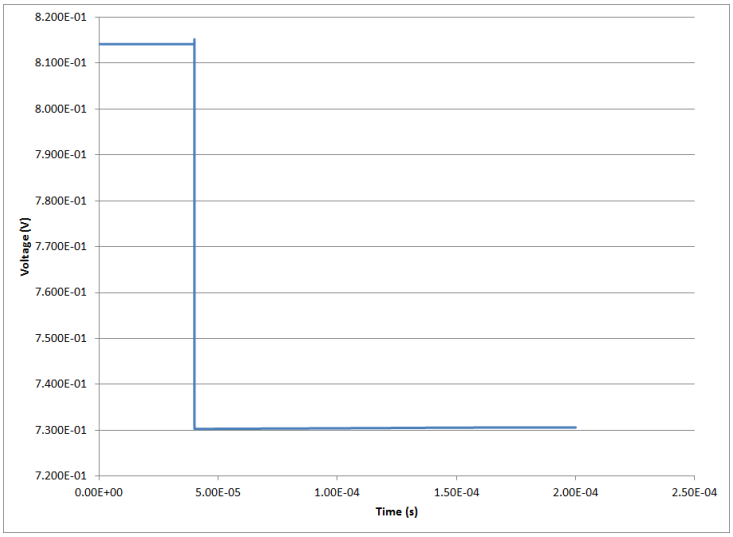

Figure 4.7: Simulated TRAPPISTe-2 CSA2 amplifier output to an input charge of ≈24000 electrons.

4.3 Amplifier Test Structures Measurement Setup

Once the operation of the amplifiers was verified by simulation, the layout of each amplifier was completed as described in 3.2.4. The standalone structures are located in the bottom left area of the chip (Figure 3.11). The bias signals were routed out to the IO ring to provide external access to the test structures. Since there was no detector implant at the amplifier input, a 37fF capacitor was placed in series at the input transistor to allow charge injection. A controlled test charge could be injected at the amplifier input with a pulse generator.

The test structures were measured using the TRAPPISTe PCB readout board which was developed for the project. The board consists of a mother board which can hold several daughter boards. The main board contains voltage and current sources to bias the test amplifiers as well as output and input connectors for connecting test equipment. The sources are controlled by an ALTERA DE2 FPGA via a PC. Via the PC, each source can be manually set to a given voltage or current.

The mother board can hold different daughter boards to accommodate different test devices and packages. KEK supplied several TRAPPISTe-2 chips which were bonded into PGA-256 packages. A daughter board was built to hold package and to interface with the main test board (Figure 4.8).

The transient response of the amplifiers was characterized with input signals generated from a pulse generator. The pulse generator was connected to the board via a coaxial cable. The places an input voltage pulse on a on-chip test capacitor to inject a known charge at the amplifiers input. The output of the amplifiers was recorded on a digital oscilloscope, which was also connected to the board with a coaxial cable.

In this manner the test structures could be characterized. The desired voltage and current settings were manually input via the PC to obtain the desired bias conditions. Then the pulse generator was programmed to give a desired input test charge. Finally the output was captured on the oscilloscope and saved to a file for off-line data processing.

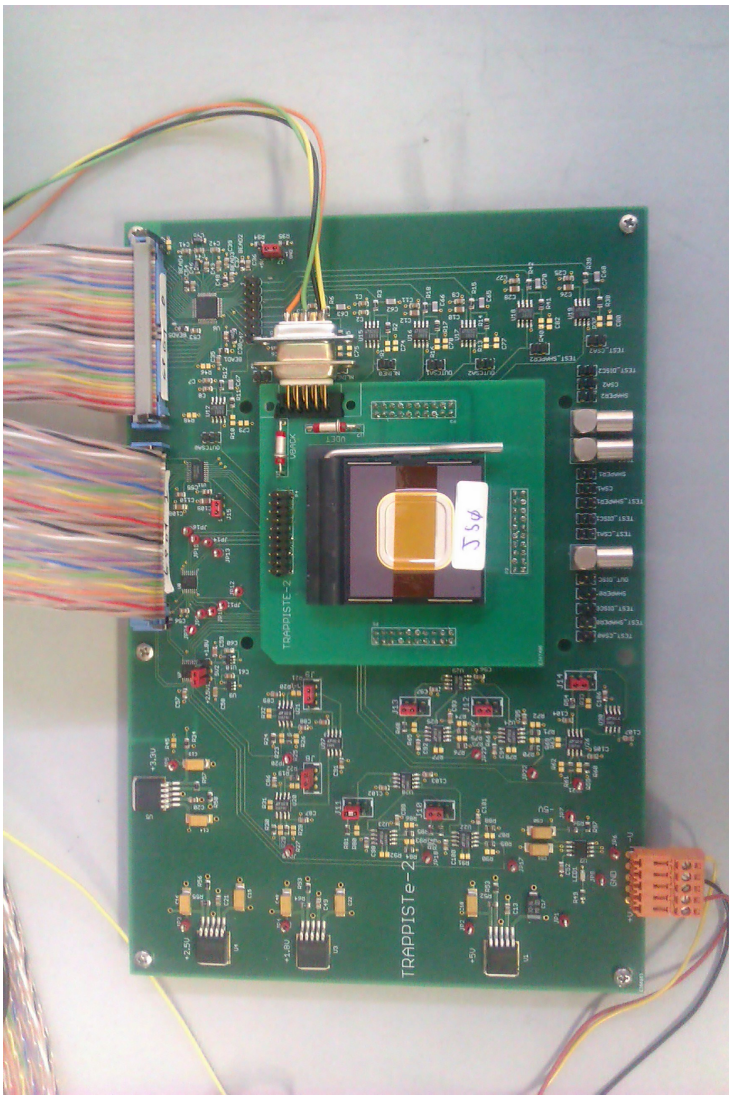

Figure 4.8: TRAPPISTe PCB with daughter board holding the TRAPPISTe-2 chip bonded in a PGA-256 package.

4.4 CSA2 Measurements

The first measurements were performed on the CSA2 test structures. As these amplifiers functioned correctly, testing was principally performed

on CSA2. The other amplifier versions CSA1 and CSA0 were also tested and their results are shown in Appendix C. The CSA2 amplifier uses the same architecture as the amplifier in the charge amplifier study, as shown in Figure 4.9. A cascode core comprised of the input transistor M1 and cascode transistor M3 are biased by several transistors. For these tests, the feedback transistor voltage V_{csarf} was set at 0.9V and the bias current I_{csa} was set at 100 μA. The value of 0.9V for V_{csarf} also provided the largest signal gain during experimental testing, as will be seen in the following tests. DC measurements were performed on the test structures to first verify the circuit operation.

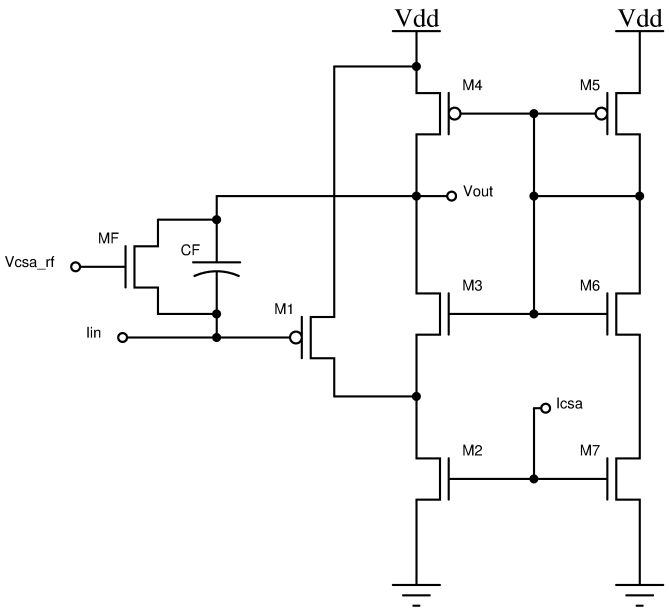

Figure 4.9: Amplifier with biasing transistors (CSA2)

4.4.1 CSA2 DC Measurements

The DC transfer curve of CSA2 was measured with an input voltage ramp placed at the amplifier input. The amplifier output in response to the ramp was recorded on a digital oscilloscope to observe the DC gain slope. The voltage on the back plane, V_{back} was varied to observe the back gate effect on the amplifiers. Figure 4.10 shows the DC transfer curve and the effect of an applied back voltage. For increasing back voltage, the output curve shifts to a lower operating point, dropping from around 0.9V at no back voltage to 0.3V at a V_{back} of 12V. Additionally, the voltage gain slope decreases from 8V/V to 3V/V as V_{back} is varied from 0V-12V, as plotted in Figure 4.11. These plots illustrate that the performance of the amplifier degrades as the back voltage increases, which will lower its effectiveness when integrated in a monolithic pixel.

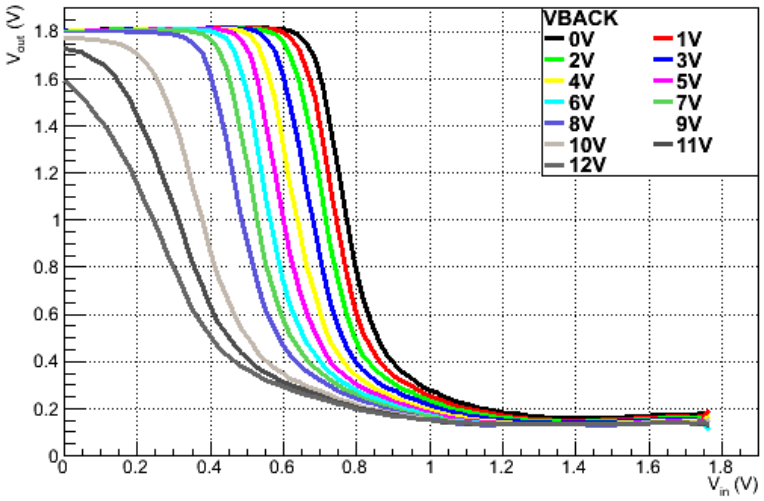

Figure 4.10: CSA2 DC response with varying back bias voltage.

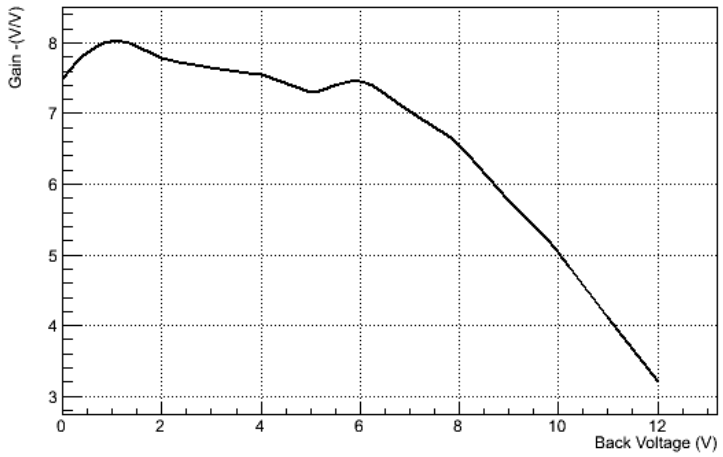

Figure 4.11: Shift in voltage gain slope for CSA2 with increasing back voltage.

4.4.2 CSA2 Transient Measurements

Transient measurements were performed by injecting a signal charge via test capacitor at the input of the circuit. A 37fF test capacitor was placed on chip in the amplifier layout. It was placed in series with the amplifier input. A voltage pulse generator was used to introduce a quick voltage pulse with risetime 2.5ns onto the capacitor, placing a known input charge at the detector input. The resulting output was captured on an oscilloscope. The test setup is illustrated in Figure 4.12. In order to observe the pulse signals, measurements were taken with the oscilloscope AC coupled. The resulting measurements were averaged over 50 triggers.

The voltage pulse on the capacitor injects a charge proportional to the amplitude of the input pulse according to $Q = CV$. Table 4.2 gives the equivalent charge for different input voltages. The equivalence in MIPs is calculated assuming a detector thickness of 300 μm of silicon. For that thickness of silicon, a passing minimum ionizing particle generates about 24000 electrons.

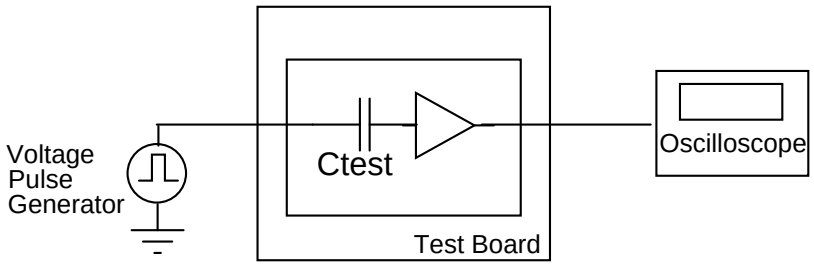

Figure 4.12: Test setup for TRAPPISTe-2 transient measurements. A voltage generator injects a input charge on a test capacitor and the output is recorded on a digital oscilloscope.

Voltage (V)	Coulombs	Electrons	MIPs
0.05	1.85E-15	1.16E+04	0.48
0.10	3.70E-15	2.31E+04	0.96
0.25	9.25E-15	5.78E+04	2.41
0.50	1.85E-14	1.16E+05	4.82
0.75	2.78E-14	1.73E+05	7.23
1.00	3.70E-14	2.31E+05	9.64
1.50	5.55E-14	3.47E+05	14.50

Table 4.2: Charge input calculation on 37fF capacitor

Figure 4.13 shows the response of CSA2 to an input voltage pulse of 0.1V which is equal to a charge injection of around 23,000 electrons. The measured signal amplitude of 64mV is less than the simulated 85mV. This can be a result of the experiment setup since parasitic capacitance at the input of the amplifier will lead to a reduction in output signal amplitude. The output voltage V is a result of an integration of charge Q of the capacitance C (i.e. V=Q/C) so any increase in the capacitance by parasitics will lead to a reduction in voltage.

During testing, any signal below around 10mV was difficult to discern from the background noise. Using the conversion factor of 64mV to 23,000 electrons, this equates to about 3600 electrons. Therefore for this test setup, the smallest detectable signal was 3600 electrons. This is a very conservative estimate and a quieter setup would be able to more

accurately determine the noise of the system. Theoretical noise values were calculated to be in the tens of electrons. In order to reach such a low level of noise measurement, special measurement setups would have to be made, perhaps battery based to avoid any power supply noise. While these levels are high compared to the theoretical levels, they are low enough to test charge collection on the order of 1 MIP.

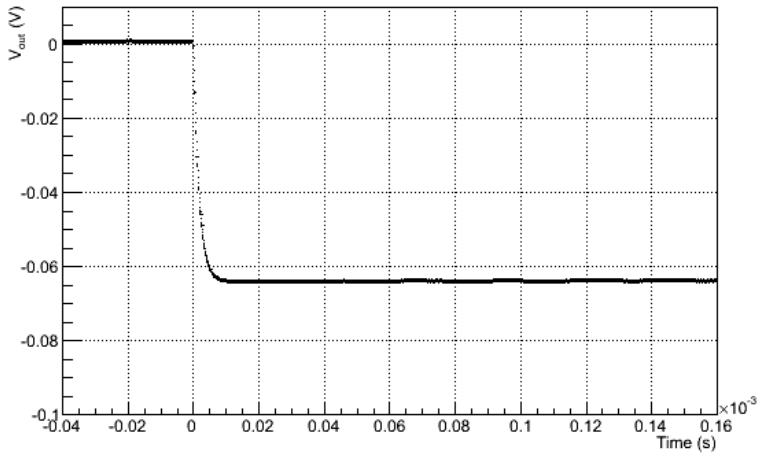

Figure 4.13: Measured CSA2 transient response to ≈23000 electrons.

In the first CSA study, it was discovered that the amplifier was quite sensitive to the feedback resistance. The feedback resistance is controlled by the voltage on the feedback transistor V_{csarf}. The response of the CSA2 amplifier to the voltage on the feedback transistor can be seen in Figure 4.14. As with the amplifier study, the TRAPPISTe-2 CSA output is also sensitive to the feedback transistor voltage. The shape of the signal changes rapidly within a few tens of millivolts of applied voltage V_{csarf}. Between an applied voltage of 1.3V and 1.0V, the falltime changes from greater than 150 μs to 10 μs.

ELDO SPICE simulations were performed to study the effect of the feedback resistance. Figure 4.15 shows the output signal at different feedback

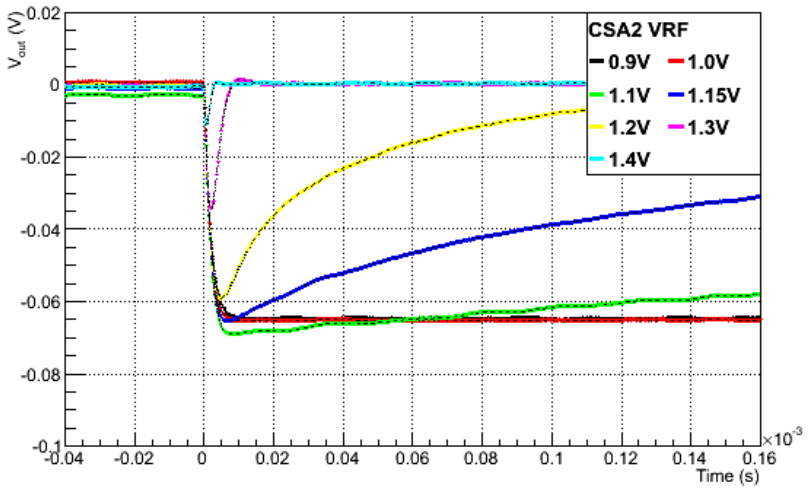

Figure 4.14: Measured CSA2 transient response with varying voltage on feedback transistor (AC coupled).

resistance values. As the feedback resistance decreases, the $R_f C_f$ time constant decreases and the output signal decays more quickly. The step voltage response is maintained for values around $10^{11}\Omega$ to $10^{12}\Omega$, then rapidly decays for lower values. Table 4.3 shows the corresponding simulated R_{ON} resistance values for a given V_{csarf} value. A standalone nMOS transistor was simulated with the same dimensions as the TRAPPISTe-2 feedback transistor (W/L = $0.7\mu m/10\ \mu m$). A small voltage of 5mV was placed across the drain and source and the gate voltage V_{csarf} was varied. The source voltage was set to 0.8V to be representative of the TRAPPISTe amplifier bias conditions. The simulated value of $10^{12}\Omega$ at 0.9V corresponds well to the observed measurements. The step response is maintained in the simulations at values around $10^{11}\Omega$ to $10^{12}\Omega$ and the measurements show a step response at 0.9V to 1.0V.

As in the amplifier study, the output capacitance of the measurement system resulted in longer measurement falltimes. For the TRAPPISTe-2 amplifier, the falltime was measured to be $5\mu s$. The coax cables used in the measurement setup could contribute as much as 200pF to the

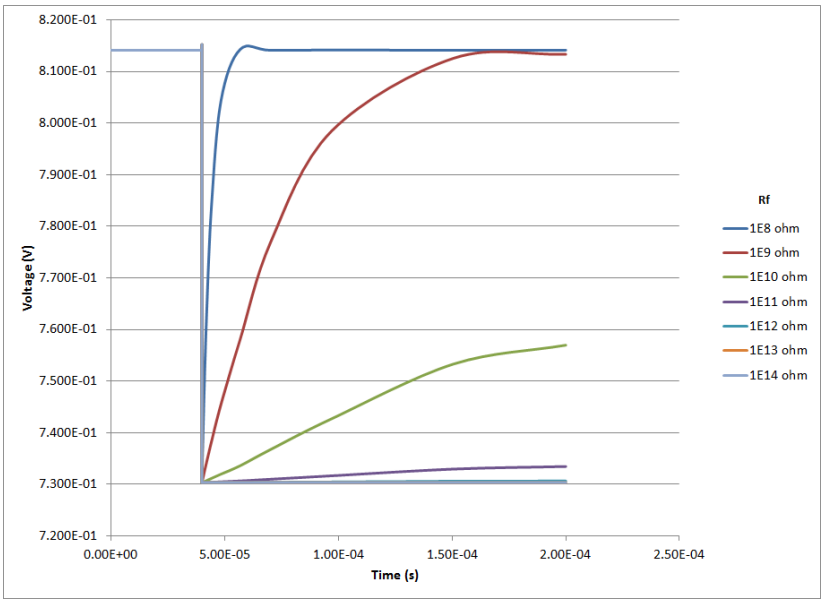

Figure 4.15: Simulated CSA2 transient response with different feedback resistance.

V_{rf}	R_{ON} (Ω)
0.8	1.0000E+12
0.9	9.9992E+11
1.0	9.9657E+11
1.1	8.7070E+11
1.2	1.3655E+11
1.4	1.4569E+08
1.6	1.9131E+06
1.8	3.7194E+05

Table 4.3: Simulated RON values for the feedback transistor

output of the amplifier. A simulation was performed with an output load capacitance of 200pF to simulate worst case parasitics. The simulated output shown in Figure 4.16 exhibits a falltime of around $5\mu s$.

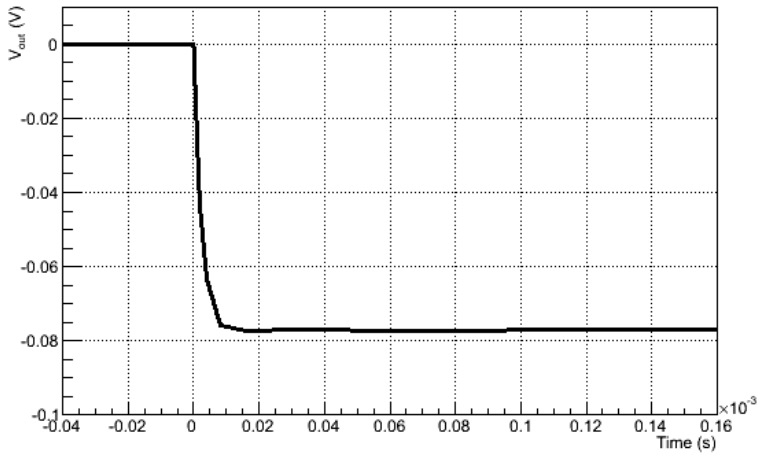

Figure 4.16: Simulated CSA2 transient response to ≈23000 electrons with 200pF load capacitance.

In the amplifier study, it was shown that the presence of a leakage current can affect the DC bias and gain of the amplifier. For the TRAPPISTe-2 amplifier, the effect of the leakage current is shown in Section 5.2.1, where the amplifier is connected to the pixel sensor.

4.4.3 CSA2 Transient Response to Back Voltage

The response of the CSA to the back bias voltage is shown in Figure 4.17 at a V_{csarf}=0.9V. The wafers for TRAPPISTe-2 have an n-type handle wafer so a positive bias was applied to the back plane to recreate the conditions of depleting a p-n diode sensor. As the back bias is increased, there is a decrease in signal amplitude and risetime. At a back voltage of 7V, the amplitude is already reduced by a third and the risetime has decreased from greater than 140 μs to 10 μs.

As with the amplifier study in Chapter 2, the effect of the back bias can be tied to the behavior of the feedback resistance. Figure 4.18 shows the evolution of the amplitude for different charge input values and shows

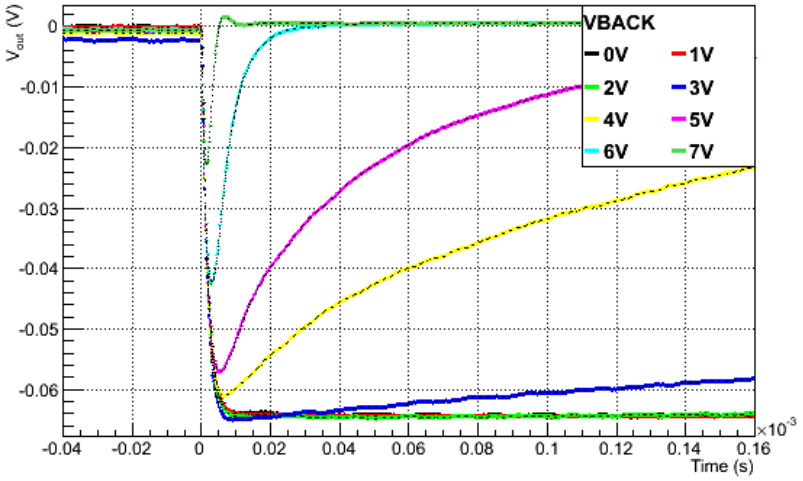

Figure 4.17: CSA2 transient response for different back voltages.

the decrease in amplitude as the back bias is increased. These curves were measured for V_{csarf}=0.9V.

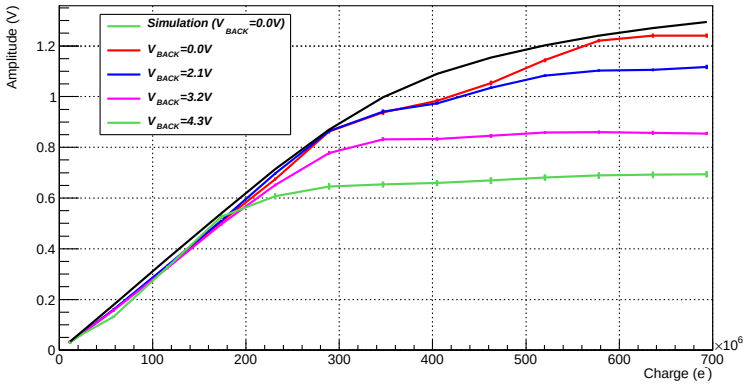

Figure 4.18: CSA2 amplitude vs charge injected for different back voltages with V_{csarf}=0.9V.

In an attempt to compensate for the effect of the back gate on the feedback transistor, the applied voltage on the feedback transistor was tuned

to try to recover the amplifier operation. This was done experimentally, by varying V_{csarf} and observing the pulse output on the oscilloscope. As the back voltage is positive, the transistors in the amplifier experience a more positive voltage on the gate area. By reducing the nominally applied voltage at the transistor gate, it may be possible to recover the nominal amplifier performance. Figure 4.19 shows how the charge curves are improved by decreasing the V_{csarf} to 0.5V for voltages V_{back} up to 8V. For higher V_{back} voltages up to 11.5V, V_{csarf} must be decreased down to 0.2V to maintain proper amplifier operation. For back voltages greater than V_{back}=12V, the V_{csarf} voltage can not be reduced enough to compensate for the back gate effect and the charge curve degrades.

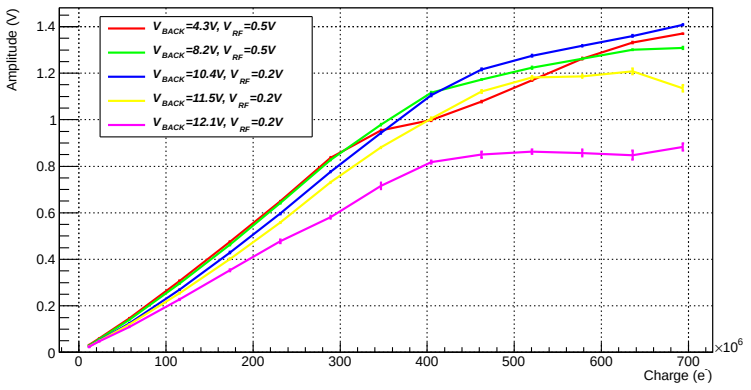

Figure 4.19: CSA2 amplitude vs charge curves can be improved by tuning V_{csarf}.

4.5 TRAPPISTe-2 Shaper Amplifiers

Due to the more advanced technology and smaller feature size of the OKI process, shaper amplifiers were included in the TRAPPISTe-2 layout. As with the charge sensitive amplifiers, stand alone test structures of the shaper amplifiers were included in the layout. The shapers were placed at the output of the CSA test structures. The shaper is a band pass

filter that transforms the step-like output signal from the CSA into a signal suitable for further pulse processing. Typical shaper amplifiers produce a semi-gaussian output signal that can be easily digitized. A standard shaper amplifier consists of a differentiating stage followed by one or more integrating stages as illustrated in Figure 4.1.

The TRAPPISTe-2 chip was designed as a proof of concept therefore a simple shaper with standard architecture was implemented in order not to complicate the design. A shaper architecture described by Jan David Schipper [93] was followed as the basis for the design. The circuit is a copy of the CSA but with a smaller input transistor and biasing transistors adjusted accordingly. As with the CSA, two versions of the shaper were produced: one with biasing transistors (SHAPER2) and one with direct biasing (SHAPER0 and SHAPER1). Figures 4.20 and 4.21 show the architecture of the shaper which is the same as that of the CSA except for a series input capacitor C_{IN}. C_{IN} acts as the differentiating stage of the shaper while the amplifier with feedback capacitor performs the role of an integrator.

Following the notes by J. Schipper [93], a 200fF capacitor is used for C_{IN} and the feedback capacitor CF is set to 50fF. The shaper is built to produce a semi-gaussian output with a shaping time of 1 μs. According to Schipper, the g_m of the amplifier does not need to be high so the input FET can be smaller and the bias current can be lower. For the shaper transistors, the size of the input transistor was reduced compared to the CSA. ELDO SPICE simulations were then performed and the sizes of the other transistors adjusted until a suitable response was obtained.

The simulated output of the shaper amplifier is shown in Figure 4.22 for Shaper2. A bias current of 28 μA is provided to the shaper. The simulation was performed with an input signal of around 24 000 electrons at the input of CSA2 which is then processed by Shaper2. The shaping time of the output is the signal width at half the maximum amplitude

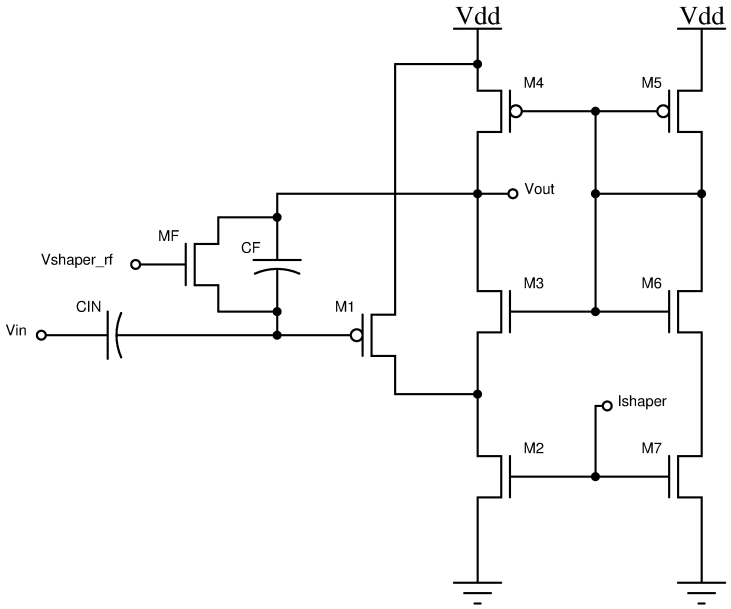

Figure 4.20: Schematic of shaper with biasing transistors (SHAPER2)

	W/L [$\mu m/\mu m$]		
Transistor	Shaper2	Shaper1	Shaper0
M1	2/1	2/2	2/2
M2	4/0.7	4/0.7	4/0.7
M3	3/0.2	3/0.2	3/0.2
M4	5/0.5	5/0.5	5/0.5
M5	5/0.5	0.63/0.6	0.63/0.6
M6	1/0.4	1/0.6	1/0.6
M7	1/0.7	-	-
MF	0.7/5	0.7/5	0.7/5

Table 4.4: TRAPPISTe-2 Shaper Transistor Dimensions

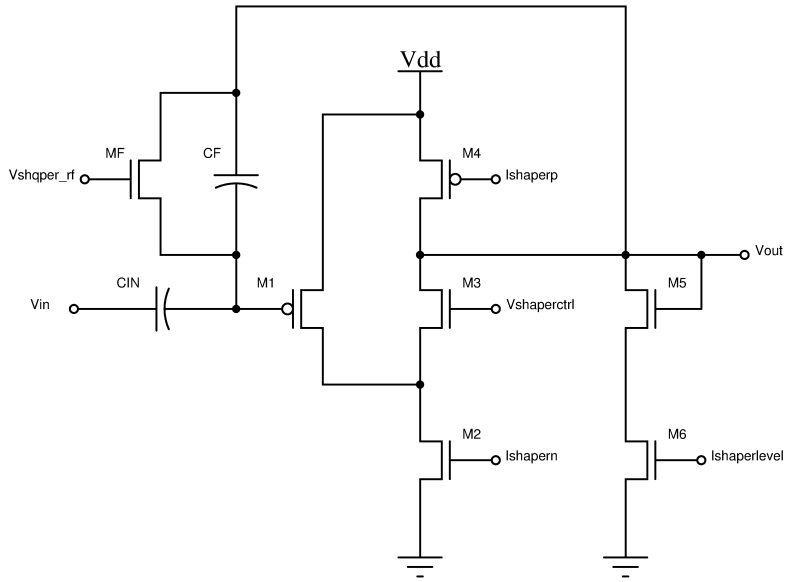

Figure 4.21: Schematic of shaper with direct biasing (SHAPER0 and SHAPER1)

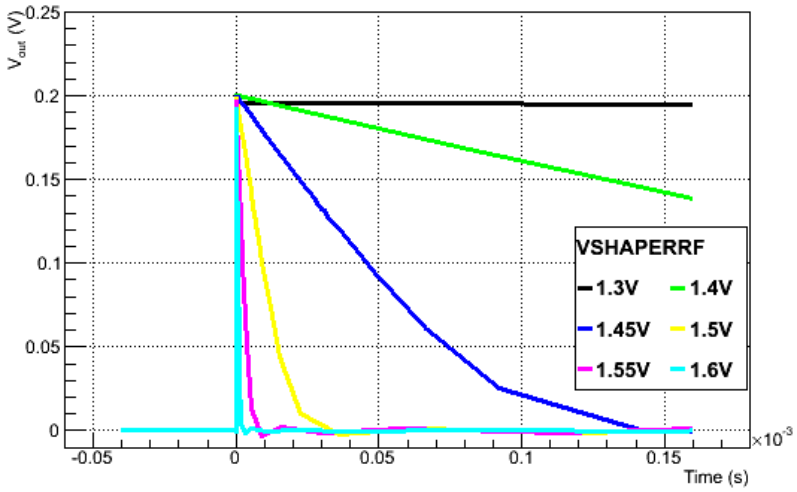

Figure 4.22: Simulated output of Shaper 2 to an input charge of 24 000 electrons. The shaping time can be controlled by the voltage on the feedback transistor.

and can be controlled by the feedback transistor. In this simulation, a shaping time of 1 μs is achieved with a feedback voltage of 1.6V.

4.5.1 Shaper2 Transient Measurements

The shaper transient measurements were made by injecting a test charge into the CSA-Shaper chain and observing the output of the shaper on an oscilloscope. The shaper should ideally amplify the CSA signal and produce a signal with a pulse width of around 1 μs suitable for digitization. The input signal to the shaper is shown in Figure 4.23. It is the CSA2 output response to a charge injection of around 23,000 electrons. Figure 4.24 shows the output of the shaper with the feedback transistor voltage V_{shaper_rf} at 1.4V and a bias current I_{shaper} of 30 μA. The location of the bias points are shown in Figure 4.20. The shaper has transformed the step-like CSA output into a semi-gaussian signal. However, the shaping

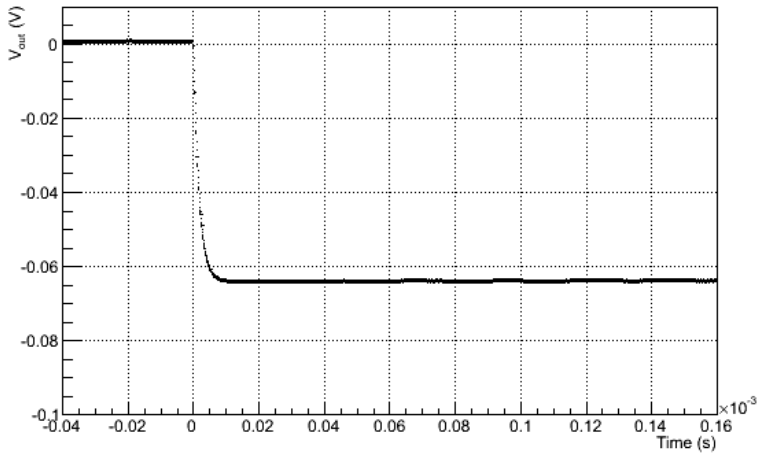

Figure 4.23: Measured CSA2 transient response with input of 23,000 electrons.

time of 30 μs is much larger than expected and the amplitude of the shaped signal is less than the CSA output.

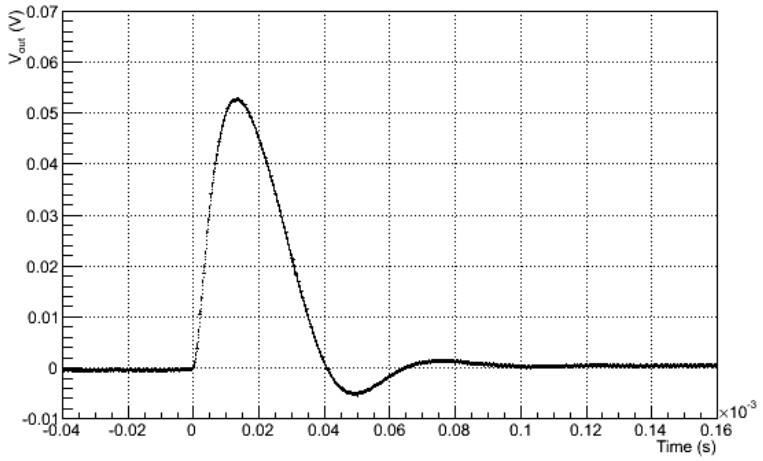

Figure 4.24: Measured Shaper2 transient response with input of 23,000 electrons.

Further analysis shows how the voltage on the feedback transistor and experiment parasitics result in the larger shaping time and reduced amplification. As expected, the shaping time of the shaper can be controlled with the voltage on the feedback transistor V_{rf} as shown in Figure 4.25. The previous simulated response shows how the shaping time could ideally be controlled down to 1 μs while maintaining the same amplification. However, the measured response shows signal attenuation as the shaping time is decreased.

The slow performance of the shaper is a result of the basic shaper that was implemented and the parasitics of the measurement setup. As TRAPPISTe-2 was a proof of concept design, a basic shaper with only one integrating stage was implemented. Additionally, the experiment setup relied on off-board connections which introduced parasitics. In order to reach the measurement equipment, 2 meter long cables had to be used. A simulation of the circuit that includes a 200pF output load capacitor representing a 2 meter long coaxial cable is plotted in Figure 4.26. The simulation shows how the parasitic capacitance slows the output risetime so that the full signal amplitude can not be reached within the desired shaping time. To avoid this problem, future TRAPPISTe

test boards should be designed with integrated readout on the PCB to avoid using off-board coaxial cables.

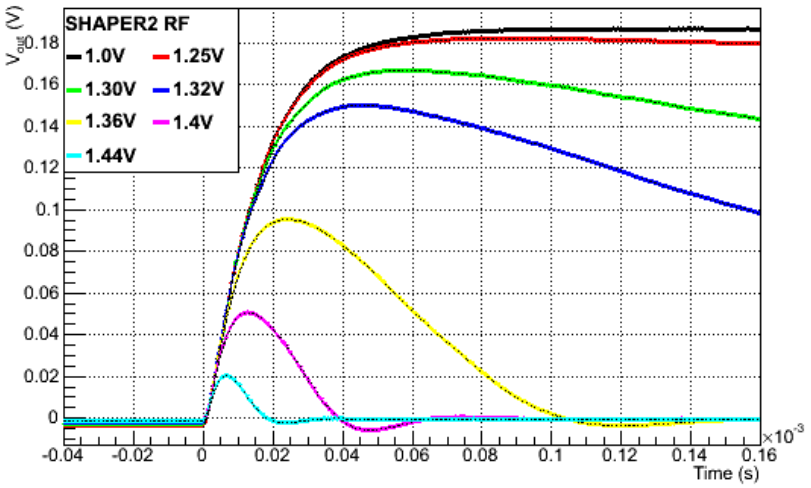

Figure 4.25: Measured Shaper2 transient response with varying V_{rf}.

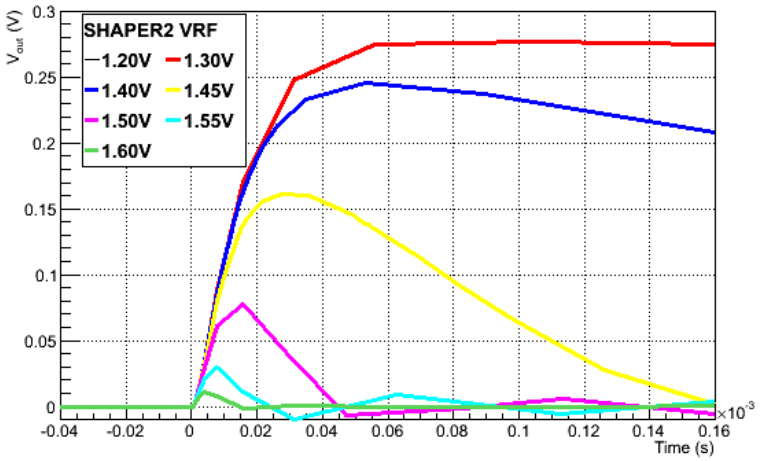

Figure 4.26: Simulated Shaper2 transient response with 200pF load capacitor.

The effect of the back bias is shown on Shaper2 in Figure 4.27 for an injection of 23,000 electrons and the feedback transistor voltage set at 1.38V. It is important to note that the applied back voltage affects both the CSA and shaper so the output curves show the decrease in signal amplitude of the whole amplifier chain. The signal amplitude is very sensitive to the back voltage, decreasing to one third of the nominal value after 2V. Results from Shaper0 and Shaper1 show similar behavior and can be found in Appendix C.

Some of the transient responses exhibit a noticeable undershoot of the signal. This can result from the long exponential decay of the charge sensitive amplifier output [95]. Many readout circuits contain a pole-zero cancellation adjustment circuit which can be tuned to mitigate the undershoot. This can often take the form of an adjustable resistance across the differentiating capacitor of the shaper. The TRAPPISTe-2 chip was designed as a proof of concept with a basic shaping amplifier which did not include any pole-zero cancellation, however this maybe considered in future TRAPPISTe devices.

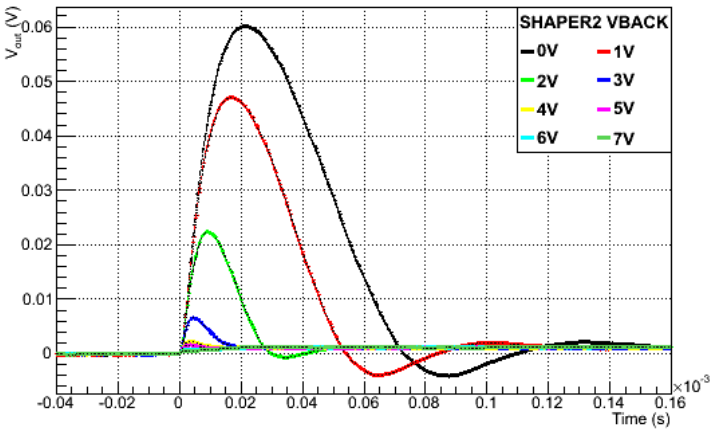

Figure 4.27: Shaper2 ouput transient response with varying Vback.

4.6 Preventing the Backgate Effect

From the measurements of the amplifier structures, it is evident that the backgate effect should be mitigated in future iterations of the TRAPPISTe chip in order to fabricate an efficient monolithic detector. Since the design of TRAPPISTe-2, several advancements in SOI detector process technologies have been made available to prevent the back voltage from interfering with the electronics in the top active layer. For example, studies by the SUCIMA project have shown that a thick active device layer can be effective against the backgate effect [96]. However, many modern sub-micron SOI processes use fully depleted thin active layers and sub-micron technologies are more desirable for detector development as they are more radiation tolerant.

In this section, three process techniques are highlighted which are available to the SOIPIX collaboration [97] and may be incorporated in the next generation of detectors, TRAPPISTe-3. These extra structures can greatly improve detector performance but at the cost of more complicated process techniques.

Buried P-well

The buried P-well (BPW) is a low dose p-implant placed underneath the buried oxide layer below the circuits to be protected, as shown in Figure 4.28. A contact to the BPW can be used to set a potential at the implant, usually ground, to shield the electronics above from the electric field in the handle wafer. The BPW can also be used to extend the sensitive area of the detector node. This technique has been shown to be effective in preventing the backgate effect in transistor tests [75]. Grounding the potential below the buried oxide also reduces the electric field in the oxide which also helps to reduce radiation damage.

However, some of the charge created by incident particles may be lost in the shielding implant, reducing the detector charge collection efficiency. In addition, studies at Fermilab have shown that fast digital signals in the top active layer can stimulate charge injection into the buried

P-well layer, mimicking a charge pulse and causing erroneous detector signals [98].

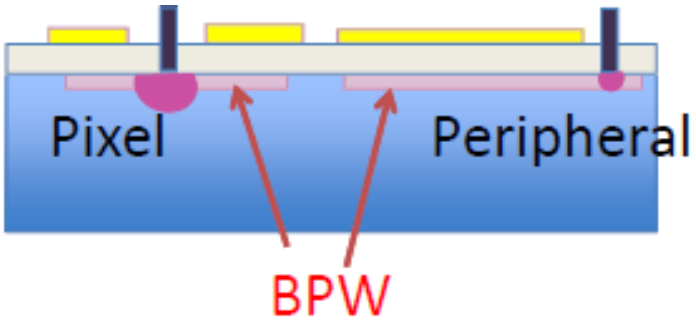

Figure 4.28: Buried P-well placed below the sensitive electronics and biased to ground [99].

Nested Wells

A more sophisticated well technology has been developed by KEK and Fermilab in conjunction with LAPIS [73]. The nested well consists of an N-well that is nested inside a buried P-well as illustrated in Figure 4.29. In this configuration, the buried P-well acts as the sensor node and the buried N-well provides the shielding to the electronics in the active layer. All the charge collected by the P-well is sent to the amplifier input. The shielding N-well also prevents interference between any digital circuits in the top layer from affecting the sensor node. However, the large implant area increases the detector capacitance which could lead to higher noise figures.

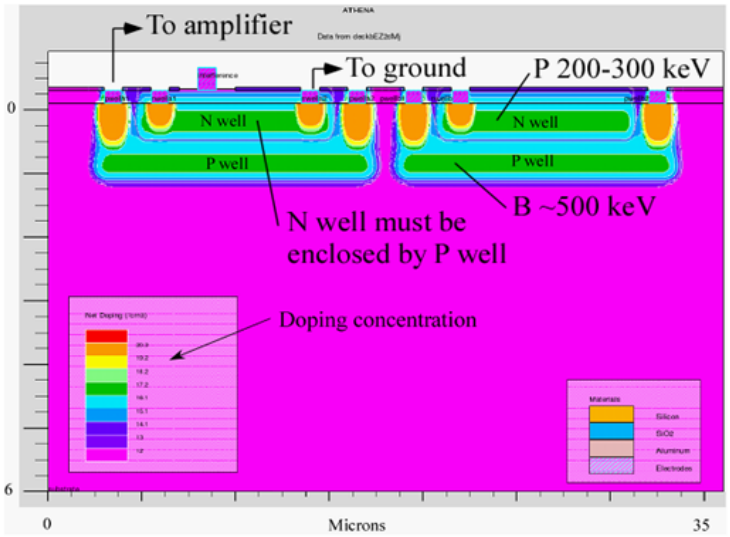

Figure 4.29: Nested well: an N-well is incorporated inside a buried P-well to isolate the electronics from the sensor node [98].

Double SOI Wafer

In addition to buried well structures, new types of SOI wafer can also be considered for future developments. A double SOI wafer has been developed by LAPIS which adds a second buried oxide and active layer on top of the usual SOI layers (Figure 4.30). For use as a monolithic detector, the detector would be developed in the bottom handle wafer and the readout electronics in the top most active layer. The middle silicon layer can be biased to act as a shield between the electronics and sensor area, preventing the backgate effect and any electronics-to-sensor crosstalk. Additionally, biasing the middle active layer may be useful in offsetting any charge build-up at the buried oxide - silicon interface during irradiation, as discussed in the following section [100].

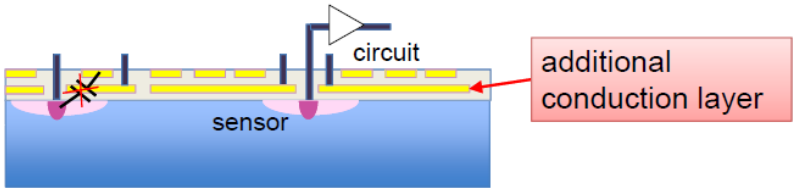

Figure 4.30: A double SOI wafer adds a second buried oxide layer and second active layer on top of the original layers [100].

4.7 Radiation and the Backgate Effect

The target application of these amplifiers is for radiation detection and therefore their tolerance to radiation effects should be taken into consideration. As discussed Section 1.7.2 in the introduction, SOI circuits have previously been used in military and space applications due to their immunity to single event effects. The buried oxide layer protects the circuitry in the active layer from induced charges created in the handle wafer as illustrated in Figure 4.31. Also, the thin active layer reduces the sensitive volume of the active devices further lowering their susceptibility to single event effects.

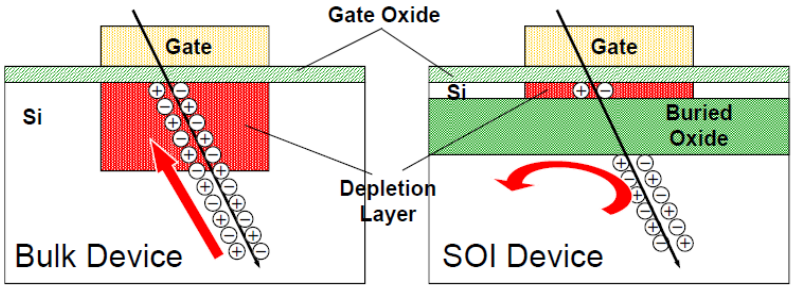

Figure 4.31: Single event effect in traditional bulk CMOS and SOI. The buried oxide layer in SOI prevents the generated charges in the handle wafer from affecting the circuits in the top layer. [101]

SOI devices are however subject to total ionizing dose effects. Passing radiation leaves behind trapped positive charges in the buried oxide layer. These charges accumulate at the oxide-silicon interface, changing the potential underneath the active devices as illustrated in Figure 4.32.

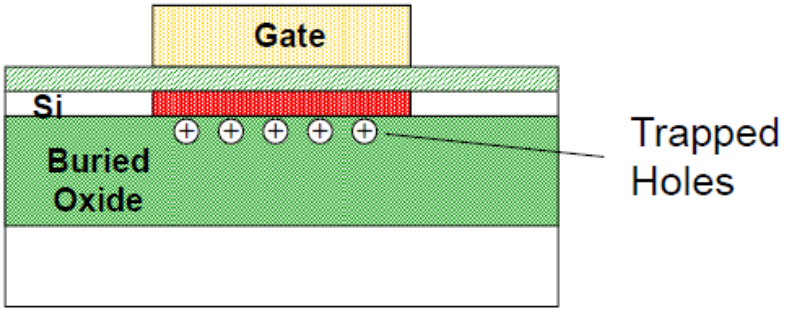

Figure 4.32: Trapped positive charge accumulates over time under increased radiation exposure. [101]

The effect of TID on OKI's 0.2um technology was measured by KEK by irradiating several transistors [102]. Transistors with and without buried P-well were irradiated with protons. It was observed that grounding the BPW was effective up to $1.3 \times 10^{12} n_{eq}/cm^2$ in preventing voltage threshold shifts but further irradiation resulted in threshold shifts.

As part of the TRAPPISTe project, standalone transistors in OKI (now LAPIS) 0.2um technology were irradiated [103]. The transistors in the TRAPPISTe-2 test area were characterized with 62MeV protons and a Cobalt-60 source. Transistors with and without a buried P-well were irradiated. The gate voltage (Vgs) versus drain current (Ids) characteristics of the transistors were measured before and after irradiation. Figure 4.33 show the effect of irradiation with 60 MeV protons on a NMOS Normal Vt transistor. The shift in the curve increases markedly after a total dose of $1.6 \times 10^{12} n_{eq}/cm^2$ with or without buried P-well present. Similar results are obtained when the transistor is irradiated with a Co60 source.

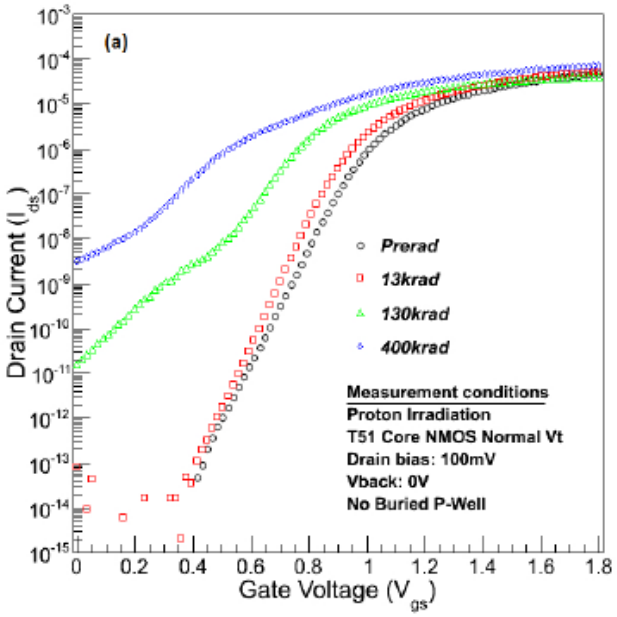

Figure 4.33: Irradiation of NMOS Normal Vt transistor with 60 MeV protons [103].

For high energy physics applications, the susceptibility to TID would be problematic. For example, the CMS tracker has a specification that the detectors should be operational up to $6 \times 10^{14} n_{eq}/cm^2$ [5]. As is, the OKI 0.2um process with buried P-well retains normal operation only up to about $1.3 - 1.6 \times 10^{12} n_{eq}/cm^2$. The transistors were not biased during irradiation. It is expected that biasing the BPW during irradiation would lower the field in the oxide and increase the chance of positive charges recombining. This would reduce the amount of built up positive charges and reduce TID effects, however this remains to be tested.

One possible solution that could pave the way for the use of SOI technology in a high radiation environment is double SOI layer technology, illustrated in Figure 4.30. The double SOI layer was previously introduced to offset the backgate effect. The detector in the handle wafer is biased with a detector bias voltage in the same fashion as in a single SOI wafer. The intermediate silicon layer could be used to deal with voltage threshold drifts due to trapped charges. The intermediate bias voltage can be set to a non-zero voltage. Tests by KEK on single SOI wafers show that this method could be effective. Figure 4.34 shows the shift in operation of transistors irradiated to $1 \times 10^{15} n_{eq}/cm^2$ by KEK [104]. This level of radiation tolerance would be enough for current particle trackers such as CMS [5]. The KEK study was performed with a 0.15nm OKI process and illustrates how radiation effects can be mitigated by biasing the back contact. In this case, nominal transistor operation could be recovered after irradiation by biasing the back voltage to -20V. In fact, if the required applied voltage can be calibrated against the received dose, a double SOI wafer may be able to act as a radiation monitor. The required back bias voltage could be used to measure how much radiation the device has been subjected to.

By biasing the intermediate conducting layer in a double SOI wafer, it may be possible to adjust for voltage threshold shifts due to radiation. Double SOI layers for mitigation against TID radiation is an ongoing subject of investigation within the TRAPPISTe project.

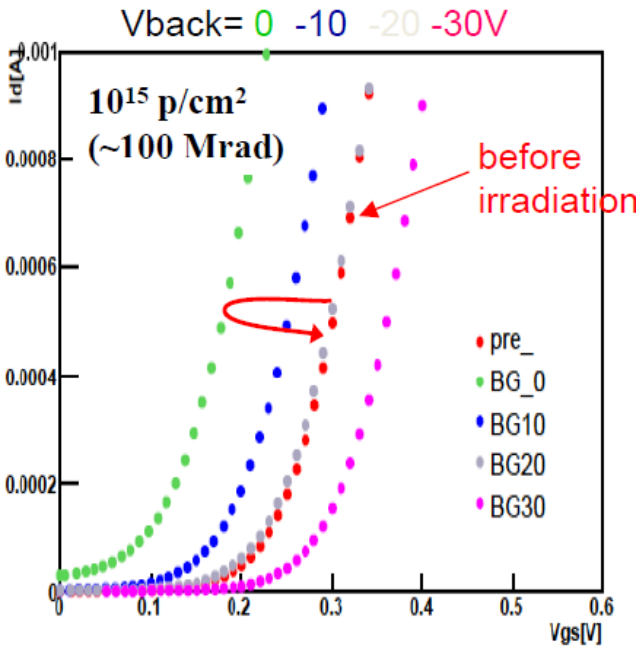

Figure 4.34: Biasing the back voltage to compensate for radiation TID effects [104].

4.8 Conclusion

A proof of concept design of charge sensitive amplifiers and simple shaper amplifiers test structures have been developed and tested on the TRAPPISTe-2 chip. These amplifiers were fabricated in an OKI 0.2 μm FD-SOI process. The test structures are standalone amplifiers which are not connected to a sensor. These test amplifiers were functionally tested to verify their response to an input charge. The performance of the amplifiers were observed under the same conditions as in a monolithic detector.

They were tested using the TRAPPISTe PCB which provided the necessary bias voltages and currents. For transient measurements, a 37fF series input capacitor was placed on-chip at the CSA input. A voltage pulse from a pulse generator was used to generate an input charge and the output of the CSA or shaper was recorded on an oscilloscope.

The CSA was based on the same design as the UCL amplifier study (Section 2). The advanced OKI technology allowed for an amplifier layout better suited for a pixel detector. A decision was made to keep the same bias of 100 μA for both amplifiers in order to re-use the same test systems so the power consumption of both amplifiers was about the same at 400 μW. However, the layout area of the TRAPPISTe-2 amplifier is 40 times smaller than the UCL amplifier (50 μm by 40 μm versus 300μm by 250μm). This allows for the creation of smaller pixels, which would have smaller detector capacitance and lower overall noise. The extra metal layers in the OKI technology also allows for more complex layout which is necessary in a dense pixel matrix. While the UCL technology may be suitable for larger pad or strip detectors, the OKI technology provides a clear advantage in building a monolithic pixel matrix.

Three variants of CSA were fabricated. CSA2, composed of low voltage transistors, used the same architecture as that described in the charge sensitive amplifier in Chapter 2. CSA1 and CSA0, composed of low voltage and standard voltage transistors respectively, contained the same cascode core as CSA2 but relied on direct biasing of transistors instead of using self-biasing transistors. All three CSA variants functioned as

expected although the measurement results were affected by experiment setup parasitics, particularly output load capacitances due to coaxial cables.

The measured output to a charge injection of 23,000 electrons (approximately 1 MIP of charge in 300 μm of silicon) was about 60mV with signal falltimes of around 5 μs for the three CSAs. With the current setup, the lowest observable pulse signal is an amplitude of 10mV which corresponds to about 3600 electrons. While the measurement setup would need to be improved to measure lower noise, this current level is low enough to detect charges down to 0.5 MIP. The ability to detect 1 MIP is an important requirement for detecting high energy particles and it has been shown that the TRAPPISTe-2 amplifier is able to accomplish this. For applications with lower noise requirements such a s X-ray detection, the measurement setup would have to be improved to show that theoretical noise levels of tens of electrons is achievable.

The effect of the back voltage on the the output is quite strong as the CSA2 and CSA1 amplitude drops to one half of its nominal value at a VBACK of 7V; CSA0 drops to two thirds of its nominal value. As seen in the charge amplifier study, the performance of the CSA under the back gate effect can be strongly tied to the feedback transistor. By lowering the applied voltage on the feedback transistor to counter the increasing voltage due to the back bias, the output amplitude of the CSA can be recovered. However, this is only possible up to a back voltage of 12V after which it is not possible to compensate for the backgate in this manner.

Basic shaper amplifiers were also characterized. The shaper amplifiers transform the step-like CSA output into a semi-gaussian output suitable for pulse processing. Three versions of the shaper with different biasing schemes were produced. Shaper2 is a self-biased amplifier composed of low voltage transistors. Shaper1 and shaper0 were directly biased amplifiers composed of low voltage and standard voltage transistors respectively. All three shaper amplifiers were functioning and the shaping time of the output signal can be controlled by adjusting the voltage on a feedback transistor. While the shapers provided a semi-gaussian output signal, the basic amplifier design resulted in long shaping times, on the

order of tesn of microseconds. In addition, parasitic load capacitances in the experiment setup also contributed to slower output responses. In addition, the measured slow signal risetimes limited the maximum signal amplitude at shorter shaping times, resulting in attenuated shaper outputs.

The back voltage effect on the shaper output is very pronounced with a decrease of signal amplitude down to one third of the nominal amplitude at VBACK=2V for all three shaper variants. It should be noted that the shaper output is the output of the CSA-Shaper chain so that the measured backgate effect is the effect on both the CSA and shaper.

These results show that the CSA and shaper amplifiers are functioning. However, exact measurements were hindered by the experimental setup used coaxial cables to connect input and output signals. In the future, a more advanced on-board measurement system should be implemented for more precise measurements. The effect of an applied back bias is quite strong. For a monolithic detector system, this means that the sensor in handle wafer can not be fully depleted lest the amplifier output be too attenuated.

Future TRAPPISTe devices will have to incorporate techniques to mitigate the backgate effect, such as buried p-well and double SOI layer techniques made available by the SOIPIX collaboration. These techniques can also help mitigate radiation effects that affect SOI devices, in particular TID charge build up at the oxide-silicon interface. Radiation tests on transistors built in OKI technology have shown that a buried P-well can be effective up to about $1.6 \times 10^{12} n_{eq}/cm^2$ [103]. This level of tolerance is not sufficient for modern particle trackers. However, techniques such as a double SOI wafer may be able to offer much higher tolerance by compensating the voltage drift with an applied bias voltage. If calibrated properly, this applied voltage could even act as a monitor indicating the level of radiation the detector has been subject to. These techniques are the subject of continued research within the TRAPPISTe and SOIPIX groups.

Despite being able to bias the TRAPPISTE-2 detector only at low voltages, the monolithic pixels with integrated amplifier readout were still tested with laser stimulation. The results are described in Chapter 5.

CHAPTER 5

TRAPPISTe-2 Amplifier Matrix

The TRAPPISTe-2 chip was developed to test the feasibility of developing a monolithic pixel detector containing a sensor and readout electronics in the same silicon-on-insulator wafer. The first step in the development was to design charge amplifiers in SOI technology as was shown in Chapter 2 using in-house UCL Technology. Second, the process steps required to turn an SOI wafer into a monolithic detector were studied using simple 3-T readout structures, first using UCL technology then in OKI technology as was described in Chapter 3. Standalone amplifiers were then implemented in OKI technology and characterized in Chapter 4. These amplifiers were shown to be functioning as expected however the backgate effect causes a significant decrease in signal amplitude. Finally, the knowledge of the amplifier design and the monolithic pixel development techniques came together to produce a pixel matrix with integrated amplifier readout in OKI technology.

The TRAPPISTe-2 pixel matrix is shown in Figure 5.1. It is a 3 row x 6 column pixel matrix with each pixel 150μm x 150 μm in size. In

the center of each pixel, a $30\mu m$ x 30 μm p-implant is created in the n-type handle wafer. The pixels on the left hand side contain an extra p-implant in the central area. The amplifiers are located in the bottom part of each pixel, connected to the the implant by metal lines and vias through the buried oxide. As with previous TRAPPISTe chips, the pixel was not covered in metal in order to allow for illumination with a laser source from the top side.

Each pixel contains an amplifier chain containing a CSA and Shaper, the same circuits as those tested in Chapter 4. Each of the three rows of the matrix contains one of the three types of CSA and shaper variants. The first row of the matrix contains the CSA0 and shaper0 type of directly biased amplifier with standard voltage transistors. The second row contains CSA1 and shaper1 directly biased amplifiers comprised of low voltage transistors. The third row contains CSA2 and shaper2 type of amplifiers which are self biased and fabricated with low voltage transistors.

Pixel size was mostly dictated by the amount of layout area available and the need to integrate an entire readout chain into a pixel.

To select which pixel to read, multiplexers were implemented, one for each row. The multiplexer is used to select which pixel structure appears on the row output as shown in Table 5.1. The multiplexers are visible on the right hand side of the matrix in 5.1. On the left hand side, bias transistors which act as current mirrors are used to provide the necessary bias currents to the pixel amplifiers.

The handle wafer in which the detector is fabricated is a high resistivity 10,000 Ωcm n-type silicon wafer with a thickness of about 300 μm. The chip backplane is biased with a positive voltage to deplete the sensor. The depletion depth W of the sensor can be estimated from

$$W = \sqrt{2\epsilon_{si}\rho\mu V} \tag{5.1}$$

where ϵ_{si} is the permitivity of silicon, ρ is the substrate resistivity, μ is the charge carrier mobility and V is the applied depletion voltage. A

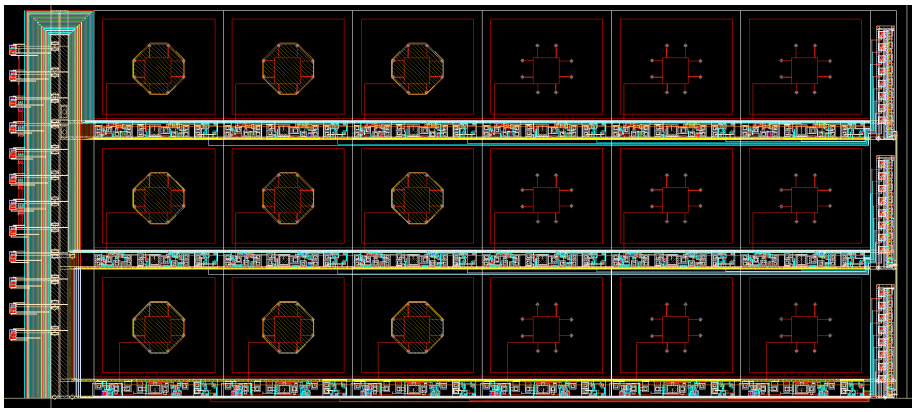

Figure 5.1: TRAPPISTe-2 pixel matrix with integrated amplifiers. Each pixel size is 150μm x 150 μm in size.

plot of the depletion width versus the bias voltage in Figure 5.2 shows that the 10,000 Ωcm handle layer with thickness 300 μm can be fully depleted at around 35V.

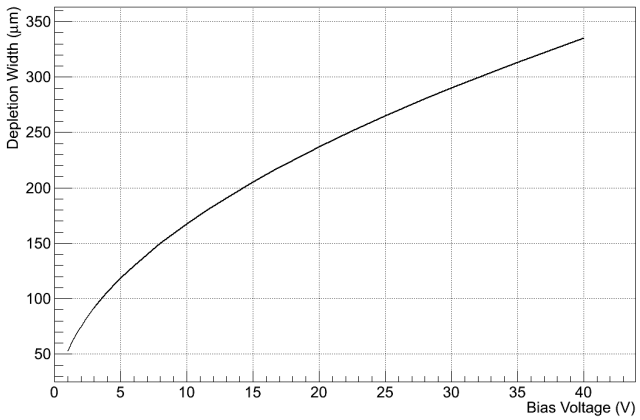

Figure 5.2: Depletion width of a 10k Ωcm silicon substrate as a function of the applied back voltage.

5.1 Laser Test Setup

The amplifier matrix was tested using the Laser for Radiation Analysis (LARA) test system. LARA was commissioned during the course of the TRAPPISTe project. The test system consists of a laser source and 3-axis motorized stage inside a sealed enclosure. LARA provides a platform to study the effect of laser illumination on test devices. For silicon sensors, this can provide a useful calibration tool as the photons from the laser can be used to inject a known charge into the sensor. One advantage of testing with a laser is that they can be tightly focused, allowing for precise targeting of the injected charge. This is important for pixel detectors, as pixel areas can be as small as a few tens of μm^2. A more detailed description of the LARA test system can be found in Appendix A.2.

For TRAPPISTe-2 testing, an infrared laser of 1060nm wavelength was installed on LARA. At this wavelength, the incident photons have an energy around 1.1eV. This energy is about equal to the silicon bandgap energy. Infrared is near the edge of the silicon absorption spectrum therefore allowing the beam to penetrate the whole of the 300um silicon. As the beam traverses the silicon, some photons will produce charge carriers while the others continue on their path. By adjusting the number of photons released by the laser, it is possible to adjust the number of electron-hole pairs created in the silicon substrate. In this manner, a MIP can be simulated by adjusting the intensity of the laser beam to generate the MIP equivalent of electron-hole pairs.

In the LARA test system, the laser intensity was regulated via the laser trigger box which is controlled by a dial with range 0-100. To estimate the approximate number of photons emitted at each laser pulse, the laser was calibrated with a fast photodiode (see Appendix A.2). The intensities mentioned in this section indicate the number of photons emitted by the laser. The frequency of the laser pulses (i.e. the number of laser pulses output per second) was controlled by an Agilent pulse generator. A diagram of the LARA setup is shown in Figure 5.3.

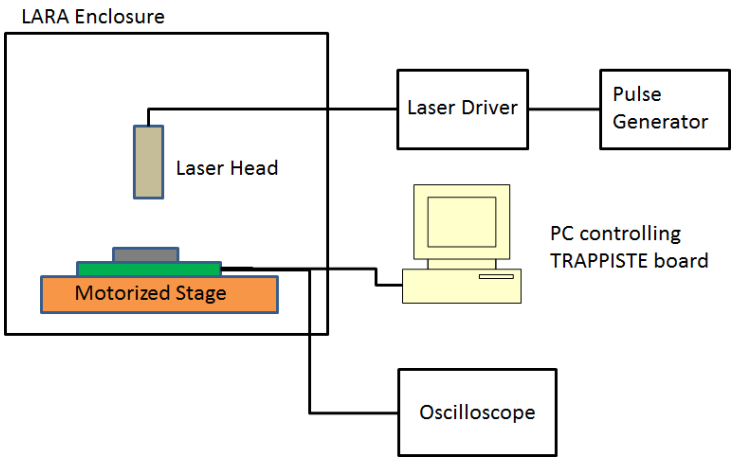

Figure 5.3: LARA setup for TRAPPISTe-2 tests. The frequency of the laser pulses is controlled by a pulse generator. The pixel output is recorded on an oscilloscope.

The laser was used to inject charges into the top side of the TRAPPISTe-2 device. The TRAPPISTe-2 chip was mounted on the TRAPPISTe PCB which provided the necessary biasing and control signals. The PCB was then mounted on a 3-axis motorized stage. The stage is remotely controlled via PC and can position the TRAPPISTe device under laser to within a micrometer accuracy. The output of the pixels was captured on an oscilloscope. A photo of the TRAPPISTe-2 device mounted on the LARA motorized stage is shown in Figure 5.4.

Matrix Readout

The TRAPPISTe-2 matrix contain 3 rows and 6 columns. Three output pads are used for the matrix readout, one for each row. These output pads are labeled OUT0, OUT1 and OUT2. The readout of the pixel matrix is controlled by multiplexers which determine which of the six pixels in the row is connected to the output pad. The multiplexers are 8-to-1 devices with three select signals select signals: Sel0, Sel1, Sel2. Table 5.1 shows the signals from the pixel matrix that can be selected.

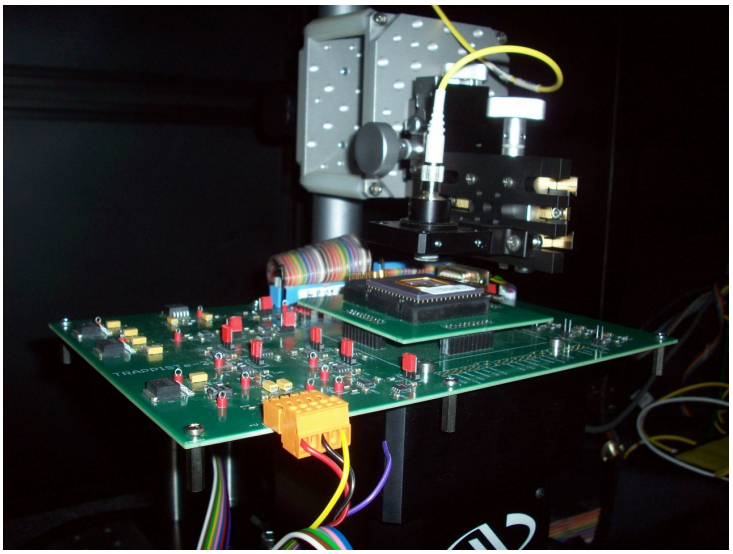

Figure 5.4: TRAPPISTe-2 test device mounted on a 3-axis stage for positioning under a laser source.

In the first five pixels, the shaper outputs of the pixels are mapped out. In the last pixel, the charge sensitive amplifier output is also accessible.

5.2 CSA Pixel Measurements

The first laser measurements were performed on the charge sensitive amplifiers. The CSA is the first amplifier in the chain connected to the sensor so their performance is critical to the overall monolithic pixel performance. The amplifiers integrated in the matrix could not be tested with a pulse source, as the standalone amplifiers in Chapter 4 were. This is because there was no way to access the input node to the CSA from the outside. Future TRAPPISTe developments may consider providing access to the integrated amplifiers input node for external charge injection. For TRAPPISTe-2, the monolithic pixels were tested directly with a laser source.

Sel0	Sel1	Sel2	Output
0	0	0	Shaper output in column 1
1	0	0	Shaper output in column 2
0	1	0	Shaper output in column 3
1	1	0	Shaper output in column 4
0	0	1	Shaper output in column 5
1	0	1	Discriminator output in column 6
0	1	1	CSA output in column 6
1	1	1	Shaper output in column 6

Table 5.1: Selection of Output via Multiplexer in Amplifier Matrix

To perform the test, the CSA output in the sixth pixel column was selected via the multiplexer and the laser was positioned over the selected pixel. A voltage (VBACK) was applied to the back metal plane of the chip in order to deplete the sensor in the handle layer. The laser was then pulsed and the response of the CSA recorded on an oscilloscope. The measurements shown in this chapter are averaged over 3 trigger signals.

As expected, no response from the amplifier was observed when no back voltage was applied as no depletion width is developed in the sensor. Only after a back voltage of around 2V was applied could a discernible signal be measured. As the signal pulses were on the order of a few tens of millivolts, the CSA parameters were tuned to achieve the largest measurable peak-to-peak signal amplitude. The settings were determined experimentally by a sweep of the bias parameters and observing the output. These amplifiers have a sensor node attached to the input which introduces leakage currents and parasitic capacitances that can give different results than the standalone amplifiers in Chapter 4. The final settings for the three CSA amplifiers are shown in Table 5.2. The bias currents and voltages for CSA2 are shown in Figure 4.2 and Figure 4.3 for CSA1 and CSA0. These bias parameters were applied to the charge amplifiers for all plots shown in this section, unless otherwise stated. In this section, the results for CSA2 are shown while the results for CSA1 and CSA0, which are similar, can be found in Appendix C.

Bias	CSA2	CSA1	CSA0
ICSAN	100 μA	100 μA	140 μA
ICSAP	-	20 μA	30 μA
ICSALEVEL	-	2 μA	2 μA
VCSACTRL	-	1.2V	1.5V
VCSARF	1.3V	1.3V	1.3V

Table 5.2: Bias parameters for the integrated pixel CSA testing. The definitions of the parameters are found in Figures 4.2 and 4.3.

5.2.1 CSA2 Pixel Measurements

The first amplifier tested was the CSA2 amplifier in the sixth column of the third row. The laser intensity was set so that each laser pulse produced around 50x10^6 photons (see calibration in Appendix A.2). This laser intensity gave a appreciable signal to measure. A beam of 50x10^6 photons produces approximately 134,952 electron-hole pairs which is approximately 6 MIPS in 300 μm of silicon. The can be calculated by from $I = I_o(1 - e^{-x/\alpha})$ where x is the silicon thickness, α is the absorption coefficient, I_o is the initial intensity and I is the intensity of the laser after traveling distance x. The silicon thickness is 300 μm for the TRAPPISTe detector. The absorption coefficient is dependent on the laser wavelength; for a 1060nm laser the absorption coefficient is 11.1cm [105].

The frequency of the laser pulses was set to a low frequency of 50Hz to allow the amplifier signal enough time to return to its base value between pulses. Figure 5.5 shows the transient output for CSA2 in response to the incident laser pulse at different values of the back voltage V_{back}. The same fall time of 5 μs is observed as was seen with the standalone test structures. However, the rise time of the signal is decreased as the signal more rapidly reaches its baseline value.

The decrease in rise time can be explained by the presence of the leakage current of the detector. The standalone test amplifiers did not have any leakage current present (or very little if a parasitic leakage current was

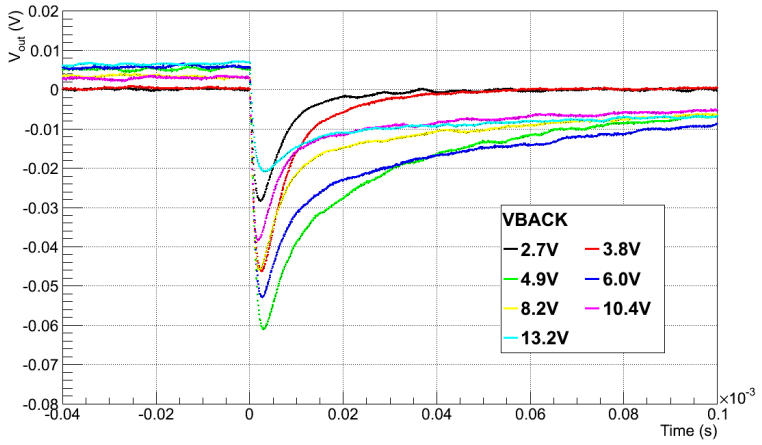

Figure 5.5: CSA2 transient response to the 1060nm laser with varying V_{back}.

present) while the integrated pixel amplifier is subject to the leakage current I_{leak} of the detector implant. As described in the first amplifier study, the presence of the leakage current will also affect the DC bias and gain of amplifier. Simulations in ELDO SPICE with the same biasing conditions show the same trend of a faster risetime slope at higher leakage currents (Figure 5.6). It is difficult however to make absolute comparisons as the measured detector output is also undergoing the backgate effect which is not taken into account by the simulation.

The effect of the back voltage can also be observed in Figure 5.5 and more clearly visualized by a plot of the peak-to-peak voltage as measured on the oscilloscope (Figure 5.7). In those plots, the laser intensity has been kept constant at $50x10^6$ photons while the back voltage is varied. The CSA is biased with 100 μA and a constant V_{rf} of 1.3V. Below a V_{back} of 2V, the sensor is not depleted enough to give a measurable signal. As V_{back} is initially increased, the depletion zone in the sensor is increased resulting in more collected charge and the amplitude of the signal increases. At these lower voltages, the backgate effect is minimal.

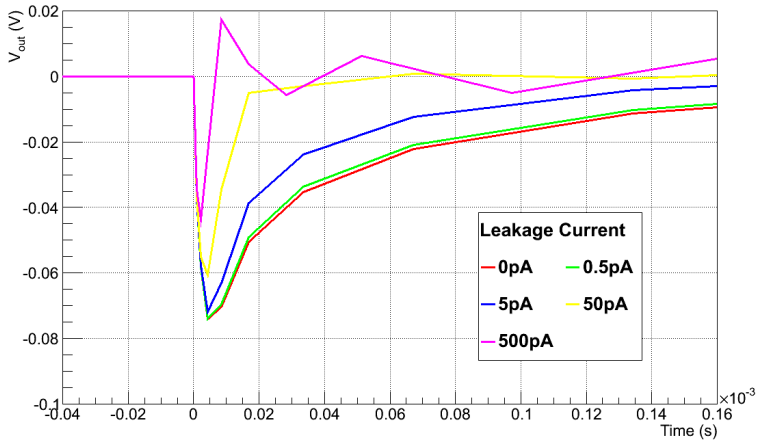

Figure 5.6: Simulated CSA2 response with leakage current and input charge of 24,000 electrons.

At around 5V, the backgate effect starts to dominate causing a quick decrease in signal amplitude despite the increasing depletion width.

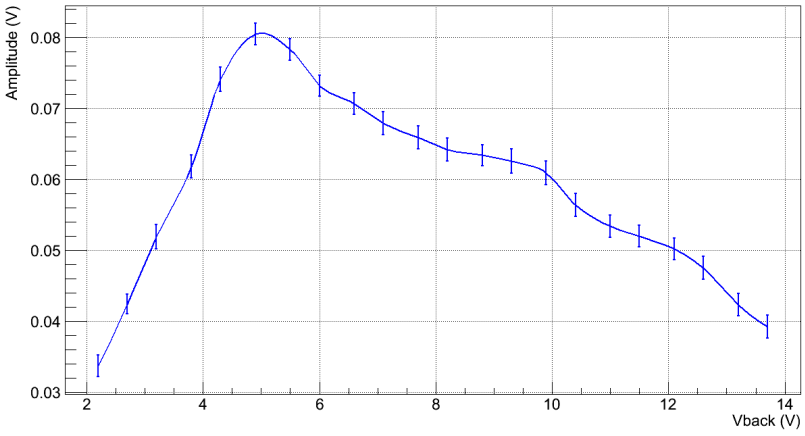

Figure 5.7: CSA2 pulse amplitude at constant laser intensity with varying V_{back}.

Subsequent laser measurements were performed at a V_{back} of 5V as the maximum signal amplitude was achieved for this back voltage. For the 10,000 Ωcm substrate, a 5V bias creates a 100 μm depletion width. Comparing the laser results to those of the the standalone amplifiers, one can look at the resulting output amplitude. The standalone amplifiers gave an output of about 64mV per 1 MIP of input charge. At 5V, a peak amplitude of about 80mV is observed. This is equivalent to about 1.2 MIP. As the sensor is only partially depleted, only a fraction of the 6 MIPS being injected from the laser is being collected. Some of the charge may also be spreading and collecting in neighboring pixels, as will be discussed further in this chapter.

Figure 5.8 shows the increase in the CSA2 output as the intensity of the laser is increased. In this plot the amplifier was biased with nominal 100 μA and a V_{rf} of 1.3V. As more photons are incident on the pixel, more charges are generated resulting in a larger output signal. The signal slowly begins to saturate for very high intensities which may result from the pixel not efficiently collecting the extra charge when a large number of incident photons are present.

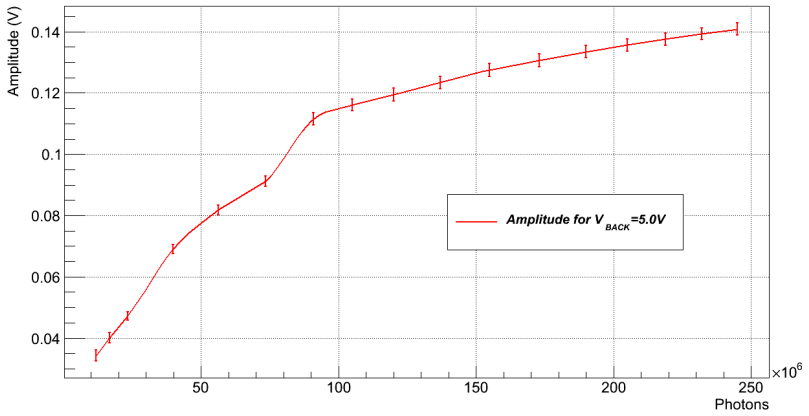

Figure 5.8: CSA2 pulse amplitude with increased laser intensity at 5V back bias.

The measurements in this chapter were taken at a slow laser pulse frequency of 50 Hz. At this low rate, the output charge signal has ample time to return to its baseline. At higher laser frequencies, the transient response of the CSA does not have enough time to recover before the next pulse arrives. As a result, a new steady state is reached in which the amplitude of the resulting signal is less than the nominal value. This is shown in Figure 5.9 where as the frequency of the laser pulse is increased, the resulting amplitude diminishes as the transient does not have time to recover before the next pulse. The recovery time of the signal is on the order of 100 μs. For a pulse frequency of 1kHz, the signal has time to fully recover. At 10 kHz, pulses occur before the previous pulse has time to recover leading to a different baseline value. At 100kHz the baseline of the signal has greatly shifted and the signal amplitude has decreased. This is important for applications which experience high rates of incident particles such as particle physics. For example, collisions at the Large Hadron Collider occur on the order of MHz [106]. The response time of the TRAPPISTe detector and readout system will have to be improved significantly if it is to be used in such applications.

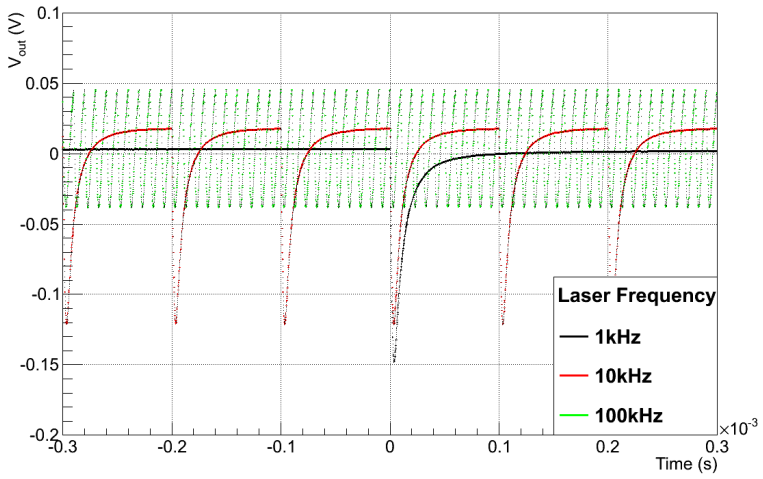

Figure 5.9: CSA2 transient response to the infrared laser with varying laser pulse frequency.

5.3 Pixel Row Measurements

The main goal of the pixel matrix is to determine the spatial position of an incident particle. To test the tracking functionality of the TRAPPISTe-2 pixel matrix, the LARA test system's motorized stage was used to target specific pixels. The laser was focused on a given pixel and the output of all the pixels in the same row were recorded. The laser was then positioned over a different pixel in the row and the measurement was repeated to observe if the pixel matrix could track the position of the laser.

As shown in the list of multiplexer outputs in Table 5.1, the main pixel outputs are the shaper signals in the amplifier chain integrated in each pixel. Therefore, measurements on the CSA-Shaper chain were first performed before the tracking measurements to characterize the shaper amplifier performance. The infrared laser was focused on the pixel in the sixth pixel column and the output from the pixels was recorded on an oscilloscope, with transient results averaged over 3 triggers. The CSA bias points were kept the same as in the previous CSA tests (Table 5.2). The shaper amplifier bias points were determined experimentally in the same way as the CSA bias point. A sweep of the parameters was made to obtain a maximum measurable signal and the results are shown in Table 5.3. These bias values were used for all shaper testing in this section unless otherwise stated.

The results of the test from the CSA2 and Shaper2 row of the matrix are shown in this section. Testing on the other two rows was also performed which yielded similar results. They can be found in Appendix C.

Bias	Shaper2	Shaper1	Shaper0
ISHAPERN	30 μA	30 μA	30 μA
ISHAPERP	-	10 μA	10 μA
ISHAPERLEVEL	-	1 μA	1 μA
VSHAPERCTRL	-	1.5V	1.5V
VSHAPERRF	1.2	1.2V	1.2V

Table 5.3: Bias parameters for the integrated pixel Shaper testing.

5.3.1 Shaper2 Pixel Measurements

Shaper2 in the sixth pixel column was the first shaper tested. The LARA 1060nm laser was set to an intensity of 50x10^6 photons and the frequency of the pulses was set to 50Hz. Figure 5.10 shows the transient response at the Shaper2 output at different back voltages. As the input to Shaper2 is the output of CSA2, the same trend with respect to the back voltage is expected. A plot of the peak-to-peak amplitude of the Shaper2 response shown in Figure 5.11 confirms this expectation. As the depletion with initially widens, more charge is collected and the output amplitude increases. At a V_{back} of about 5V, the backgate effect dominates, resulting in decrease in amplitude. As the maximum response was found to be at 5V, subsequent measurements were performed with V_{back}=5V.

Shaper2 Pixel Targeting

With the functioning of the Shaper confirmed, tracking of the laser could be measured. The laser head was first positioned over the pixel in column 1 and the shaper outputs of all the pixels in the same row were recorded. The laser was then positioned over the pixel in the fourth column with the measurements redone and then lastly the sixth column. Figures 5.12 to 5.14 show the response of the pixel row as the laser is positioned over the pixel in the first column, the fourth column and the sixth column respectively. One can see that the targeted pixel exhibits a signal 3 times

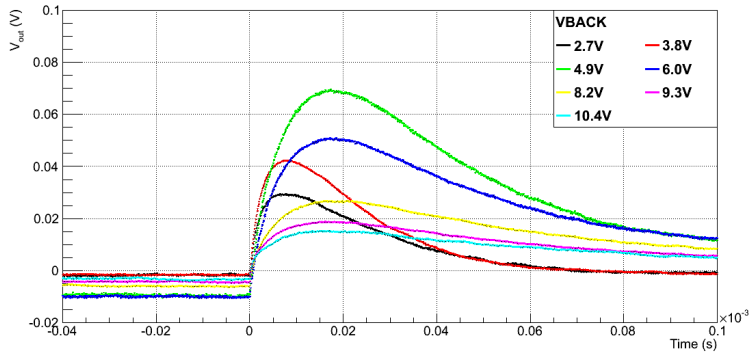

Figure 5.10: Shaper2 transient response to the 1060nm laser with varying V_{back}.

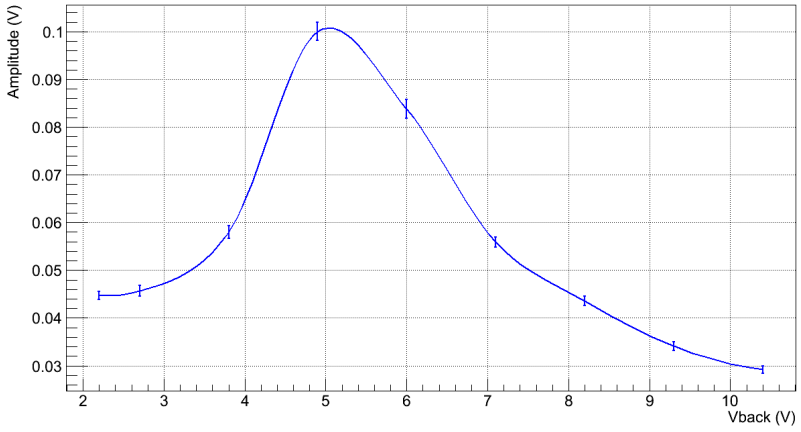

Figure 5.11: Peak-to-peak amplitude response of Shaper2 to the 1060nm laser with varying V_{back}.

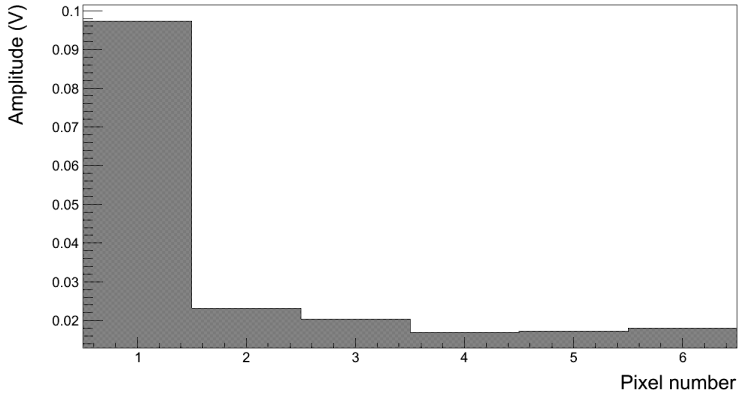

Figure 5.12: Pixel response with laser centered on pixel in column 1.

larger than the other pixels, which allows for a basic determination of the laser position.

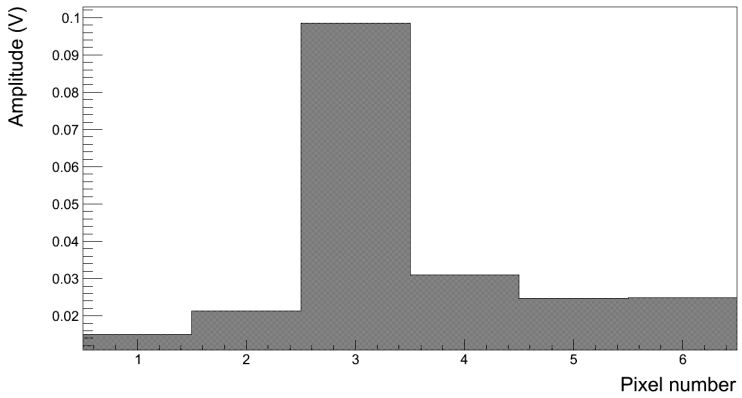

Figure 5.13: Pixel response with laser centered on pixel in column 3.

From the targeting figures, the neighboring pixels closest to the targeted pixel show larger signals than pixels further away. Several factors may contribute to this measurement with one main factor being the partially depleted detector. As only 5V is applied to the detector, the deple-

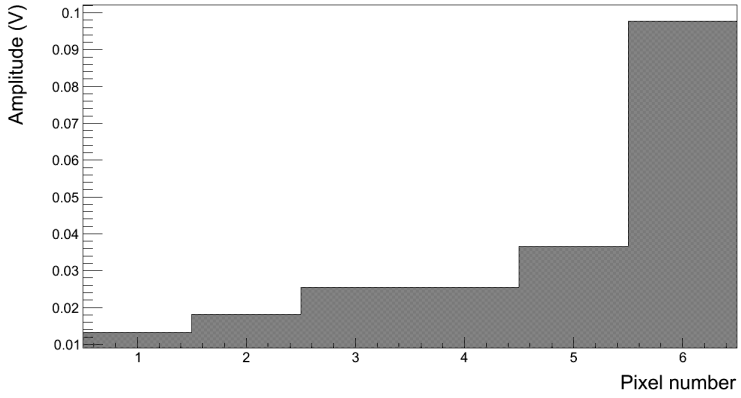

Figure 5.14: Pixel response with laser centered on pixel in column 6.

tion width is about $100\mu m$ leaving $200\mu m$ undepleted. Charges that are generated in the undepleted region will drift randomly since there is no induced electric field. This random drift can lead to charge being induced in neighboring pixels. While the charges created in the undepleted substrate will eventually recombine, the high purity silicon substrate (10,000 Ωcm) means charges may travel further before recombining.

In order to achieve full depletion of the sensor area, the backgate effect would have to be stopped. As discussed in Chapter 4, a double SOI wafer could provide a sensor which is isolated from the readout electronics. With a fully depleted sensor and electronics, one could expect that the crosstalk between pixels would be significantly reduced. From the preliminary results with a partially depleted sensor, a targeted pixel could be identified therefore one could expect that a matrix with a resolution of at least one pixel size could be implemented with a fully depleted sensor. However, this is to be verified in future TRAPPISTe devices.

The test setup itself can also contribute to the perceived spreading of the signal. The accuracy of the laser position, the focus of the laser beam and diffraction of the beam could all add to a spread out signal.

The accuracy of the LARA laser positioning within a pixel could lead to charge sharing with neighboring pixels. In general, the laser was

positioned over each pixel by dead reckoning. As there was no visual feedback to the laser position, the laser was moved 300 μm relative to its position in the previous pixel. This could cause the laser being positioned slightly more to the left or right of centre within the pixel, increasing the chances of charges being collected in neighboring pixels. Future upgrades of the LARA test system will include a camera in order to facilitate pointing of the laser.

The spread in the focus of the laser beam may also contribute to the spreading of the signal to neighboring pixels. A plot of the beam size of the laser at different distances between the device and laser head is shown in Figure 5.15. This data was provided by Masters students Geoffrey Alexandre from the Universite catholique de Louvain and Simon Kuitenbrouwer from the University of Antwerp. While the minimum achievable beam diameter is $5\mu m$, a shift of position of just 1.5mm closer to or further from the laser results in a beam diameter close to $50\mu m$ which is already one third the length of a pixel. The uncertainty in laser position and beam size all contribute to the uncertainty the tracking measurement.

In addition to the beam spread, diffraction occurs as the beam leaves the optical fiber. This diffraction results in regions around the central beam spot being illuminated and therefore generated charge.

5.4 Conclusions

A monolithic pixel matrix in Silicon-on-Insulator technology was developed on the TRAPPISTe-2 chip. The proof of concept pixel matrix contains a small three row by six column matrix with integrated charge amplifiers. The size of the TRAPPISTe-2 pixels, $150\mu m \times 150\mu m$ is on par with current hybrid detectors used in the CMS detector (150 μm $\times$ 100 μm) and the ATLAS detector (50 μm $\times$ 400 μm). Preliminary measurements show that it is possible to track a laser source pointed at a given pixel though the limited bias voltage resulted in a large amount of crosstalk. A targeted pixel displays a signal about three times larger

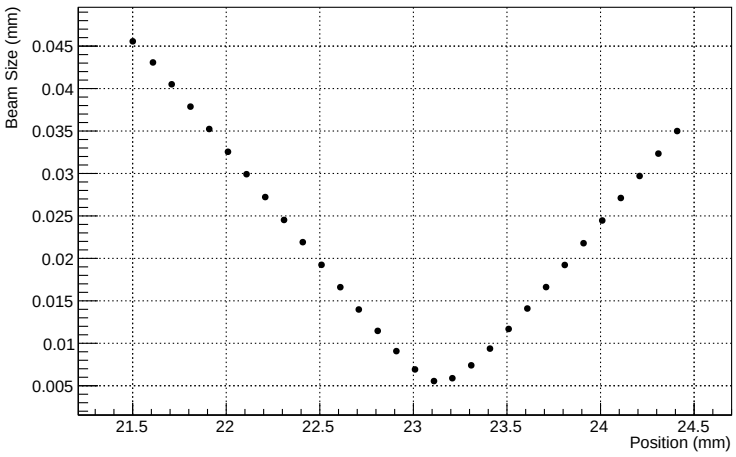

Figure 5.15: LARA laser beam size vs z-axis position.

than the two neighboring pixels. At an absolute worse case, one could say that the resolution of the matrix is about three pixels wide. One would expect that with a fully depleted sensor region and properly shielded readout electronics that the crosstalk would be significantly reduced and that a resolution of at least one pixel size could be achieved, however this is still to be proven.

This monolithic pixel matrix was the culmination of standalone amplifier studies and studies on how to integrate a sensor into an SOI wafer. Each row contains a variant of the standalone amplifiers measured in Chapter 4: row 1 contains CSA0 and Shaper0, row 2 contains CSA1 and Shaper1 and row 3 contains CSA2 and Shaper2. Previous tests were performed these amplifier test structures without a detector attached using an input test charge. With the integrated pixel matrix, the amplifiers are connected to a pixel detector in the SOI handle wafer.

An infrared laser source at 1060nm was used to inject charge carriers in the pixel substrate. The amplifier response was captured and recorded on an oscilloscope. Measurements with the laser source show how the back voltage causes an interplay between the depletion width and the backgate

effect. As the back voltage is increased initially, the depletion width increases and more charge is collected resulting in an increased amplifier output. At the same time, the backgate effect shifting the operation of the transistors causing decrease in signal output. Figures 5.11, C.17 and C.18 show how after around 5V of applied voltage, the signal increase due to the widening depletion region is offset by the backgate effect. At lower voltages, the backgate is less pronounced however as the back voltage increases it dominates the output response. All three amplifiers exhibited the same response to the back voltage.

Further testing was done with an applied voltage of 5V as this provided the largest response. For the 10,000 Ωcm handle layer substrate, this results in a depletion width of 100 μm. A comparison with the standalone amplifiers showed that when 6 MIPS of charge was induced by the laser, only about 1.2 MIPS was being collected. The laser was positioned over a given pixel and the output of all the pixels in the row were observed. The measurements such as those shown in Figures 5.12, 5.13 and 5.14 show that the targeted pixel displayed a response 2-3 times higher than the other pixels. While the results show that rudimentary position tracking of the laser is possible, there is a significant amount of crosstalk between pixels. This crosstalk is likely the result of many factors. The partially depleted handle wafer means that charge from the laser is being generated in an undepleted region. As there is no induced electric field in this region, the generated charge will move randomly and can induce charge in neighboring pixels. Diffraction from the beam aperture and the uncertainty in the beam's position and width can also lead to charge appearing in nearby pixels.

This proof of concept is a promising result for future iterations of the TRAPPISTe chip. Integrated pixels, with sizes representative of current modern particle detectors, have been developed in SOI. However, improvements are needed with regards to the circuit degradation due to the back bias. The circuit degradation limits the amount of voltage that can be applied to the substrate which in turn limits depletion width of the sensor. For more efficient and reliable charge collection, the sensor in the substrate should ideally be fully depleted to a depletion width of

300 μm. This would increase the signal of the targeted pixel and allow for a higher signal ratio compared to neighboring pixels. Preventing the backgate effect is the first step in achieving this goal, as it would allow the sensor to be fully depleted without degrading the amplifier performance. The next iteration in the TRAPPISTE project, TRAPPISTe-3, will incorporate techniques such as those discussed in 4.6 to mitigate the backgate effect and improve the performance of the TRAPPISTe chip.

CHAPTER 6

Conclusion

The TRAPPISTe project began in 2008 as a research and development project to study the feasibility of developing a monolithic pixel detector for particle tracking in silicon on insulator technology. Starting from that concept, several proof of concept devices were developed. Standalone charge amplifiers in UCL technology were first studied. These amplifiers were then incorporated into the TRAPPISTe-2 chip built in OKI technology as part of the SOIPIX collaboration. TRAPPISTe-2 contains several test amplifiers as well as a small monolithic pixel matrix with integrated readout electronics. Along with the development of the devices, readout boards were designed and a laser system was commissioned to study charge collection. Measurements performed on the TRAPPISTe-2 chip demonstrate that:

- Monolithic pixels with integrated sensor and charge sensitive amplifier can be built in SOI technology
- The charge amplifiers are able to detect less than 1 MIP of injected charge

- The size of the integrated pixels, $150\mu m \times 150\ \mu m$, is of the same size as with current state of the art pixels used in particle trackers
- Stimulation with a laser source shows that the pixels are responsive to charge injection and to the position of the laser

The TRAPPISTe project began with a charge amplifier study in UCL technology. A standalone amplifier was tested in UCL technology, then the same architecture was used for the TRAPPISTe-2 amplifiers. The advanced OKI technology on TRAPPISTe-2 allowed for an amplifier layout better suited for a pixel detector. A decision was made to keep the same bias of 100 μA for both amplifiers in order to re-use the same test systems therefore the power consumption of both amplifiers was about the same at 400 μW. However, the layout area of the TRAPPISTe-2 amplifier is 40 times smaller than the UCL amplifier (50 μm by 40 μm versus $300\mu m$ by $250\mu m$). This allows for the creation of smaller monlithic pixels, which would have smaller detector capacitance and lower overall noise. The extra metal layers in the OKI technology also allows for more complex layout which is necessary in a dense pixel matrix. While the UCL technology may be suitable for larger pad or strip detectors, the OKI technology provides a clear advantage in building a monolithic pixel matrix such as TRAPPISTe-2.

The focus of the TRAPPISTe-2 chip was to successfully integrate a charge amplifier monolithically into a pixel. A monolithic detector provides an advantage over current state of the art hybrid detectors by reducing material costs and eliminating the need for expensive and complicated bump bonding techniques. The TRAPPISTe-2 detector contains a $300\mu m$ thick sensor with readout incorporated on the same wafer. Pixel detectors in the CMS and ATLAS detectors at the LHC have $300\mu m$ [30] and $250\mu m$ [31] thick sensors respectively but then have an additional material cost of a readout wafer bonded to the sensor wafer. SOI technology also has some benefits over other MAPS technologies. For example, SOI circuits can take advantage of full CMOS circuits as opposed to epitaxial layer detectors which only use nMOS transistors [56]. While other MAPS technologies such as DEPFETs [54] and HV-CMOS [57] contain thin depletion layers on the order of tens of microns, SOI wafers have

the potential to contain depletion layers of a few hundred microns which can collect more charge. SOI wafers can also be combined with Through Silicon Via (TSV) technology to create 3D circuit devices [58]. The first layer of a such a 3D device could contain a sensor with charge amplifier like TRAPPISTe. This could then be integrated via TSV technology with another layer containing more advanced readout circuitry to create a complete detector system.

In terms of layout area, the size of the TRAPPISTe-2 pixel at $150\mu m$ $\times$ $150\mu m$ is representative of current state of the art pixels. The hybrid detectors used in the CMS detector are 150 μm $\times$ 100 μm in size [30] and the ATLAS detector uses 50 μm $\times$ 400 μm sized pixels [31]. The TRAPPISTe pixels could be made smaller as currently the amplifier readout takes up one fifth of the whole pixel size. The layout area of only the charge amplifier is 50 μm by 40 μm. Comparisons with other monolithic technologies is difficult as many monolithic technologies use 3T readout due to technological limitations or optimization for a given application. HV-CMOS is one technology that has also incorporated some proof of concept charge amplifiers in a pixel. Studies for future ATLAS detectors have developed simple charge amplifiers with a discriminator output that fit within a $33\mu m$ by $125\mu m$ pixel [57]. The TRAPPISTe amplifier could be accommodated in a pixel that size.

TRAPPISTe-2 was built as a proof of concept device. While it has shown the viability of implementing a charge amplifier in a monolithic pixel detector in SOI technology, there are improvements to be made for future TRAPPISTe devices in terms of radiation tolerance, noise, speed and power.

While immune to single effect effects, SOI wafers are susceptible to total dose effects due to the buried oxide layer. Radiation tests on OKI technology devices have shown that transistors are resistant to radiation up to about $1.6 \times 10^{12} n_{eq}/cm^2$ [103]. High performance particle physics experiments may experience up to $6 \times 10^{14} n_{eq}/cm^2$ of radiation however [5]. Potential solutions exist to improve radiation resistance, one of the most promising being the double SOI wafer (see Section 4.7). A double SOI wafer contains and extra oxide and silicon layer in the wafer. The middle

silicon layer can be biased to offset any threshold shifts introduced by radiation exposure. It may even be possible to monitor the total amount of radiation received by observing the bias required to restore circuit operation.

Theoretical noise calculations showed that a $150\mu m \times 150\ \mu m$ pixel such as that implemented on TRAPPISTe-2 could go as low as a few tens of electrons of noise. However, the current TRAPPISTe measurement setup consists of a PCB to bias the chip but all measurements are taken off the PCB with coax cables. With the current system, the smallest detectable pulse signal is on the order of 3600 electrons. This level allows for MIP detection but would be problematic for lower noise applications such as X-ray detection. Theoretical noise limits are on the order of tens of electrons however so it X-ray detection can be possible if the appropriate test setup and readout is designed. The CMS pixel tracker readout exhibits approximately 270 to 430 electrons of noise depending on the readout mode [30]. The MIMOSA series of monolithic detectors has reported achieving noise down to 14 electrons [94]. In order to detect noise down to the theoretical noise figures of tens of electrons for TRAPPISTe would require more specialized measurement techniques. These measurements could be improved by building more integrated test systems and implementing output buffers and filters.

The measurement setup also hindered the characterization of the speed of the amplifiers. Simulated TRAPPISTe-2 signal fall times were 100ns but measurements were on the order of 5 to 10 μs. This was in large part due to the measurement setup which relied on off board cables connected to measuring equipment. As with the noise measurements, an on board integrated test system would provide better speed characterization. State of the art pixel readout systems used in the Large Hadron Collider are able to achieve 50ns readout times in order to deal with particle events generated every 40MHz [30].

The TRAPPISTe-2 was biased with a current of 100 μA for a total power consumption of about 400 μW. This bias current was chosen so that the same readout board could be used across different TRAPPISTe chips and can be improved. Current state of the art hybrid detector systems

such as CMS, where low power consumption is critical due to having to power millions of pixels, allocate 34 μW for readout per pixel [30]. While many of the monolithic pixel detectors currently being developed use 3T readout structures, initial studies of HV-CMOS pixels developed for future ATLAS upgrade have developed simple charge amplifiers with a discriminator output that use 7 μW of power per pixel [57].

The first TRAPPISTe devices have shown the viability of creating a monolithic pixel sensor in SOI technology. A pixel matrix with $150\mu m \times 150\ \mu m$ pixels was created with integrated sensor and readout electronics. The matrix was responsive to charge injection by a laser with the ability to track the position of the incident beam. These first devices have also highlighted the detrimental effects of the backgate effect in a monolithic SOI device. The backgate effect significantly degrades the operation of the readout circuitry and hinders the efficiency of the sensor by limiting the sensor biasing voltage and depletion depth. In order to realize the full potential of SOI technology for pixel matrices, techniques such as buried wells and double SOI wafers will have to introduced.

Once the backgate problem has been solved, monolithic SOI detectors can leverage the use of full CMOS circuitry, small pixel size and low noise levels for use in several potential applications. Several of these applications are being pursued within the SOIPIX consortium [107].

- Particle tracking in high energy physics experiments: Pixel sizes can be made as small as or smaller than current state of the art particle trackers and with everything on one wafer, material costs can be lowered. The TRAPPISTe detector is designed as a tracking detector. Also, an SOI detector called PIXOR is in development for the BELLE II Vertex Detector [108].

- X-ray detection: Low noise levels make it possible to use SOI detectors for x-ray detection. The SOPHIAS detector has been developed for the SACLA electron free laser facility [109].

- X-ray astronomy: SOI circuits have been regularly used for space applications due to their SEU immunity. The XRPIX is an SOI detector used for X-ray astronomy on a satellite [110].

- General purpose counting: Monolithic SOI detectors can be developed for general event counting with all the required readout integrated with the sensor. The CNTPIX detector is a counting detector by KEK [72] and the MAMBO counting detector has been researched by Fermi National Labs [73].

Future TRAPPISTe Work

The results of TRAPPISTe-1 and TRAPPISTe-2 highlighted the detrimental affect of the backgate voltage on the operation of a monolithic detector in SOI technology. Further developments in the TRAPPISTe project will concentrate on mitigating the backgate effect in order to build a viable monolithic detector. The SOIPIX collaboration has been researching several different techniques to prevent the back bias from affecting the circuitry in the top active layer as detailed in Section 4.6. Buried p-wells and nested wells with n-wells within p-wells may provide a solution. These extra wells are placed in the handle layer underneath the active circuits and are biased at 0V to create a shielding effect. While effectively shielding the circuit, these extra implants may divert induced charges away from the sensor, lowering the efficiency of the detector. Also, these extra layers require more involved process techniques, complicating the fabrication process.

Another possible solution is the use of double SOI wafers. These wafers contain an additional buried oxide layer and silicon layer. The top most silicon layer can be used to develop the readout circuitry and the handle wafer would contain the sensor, as in a regular SOI detector. The middle silicon layer can be biased to act as a shield between the sensor and electronics and can also be used to offset total dose radiation effects. If calibrated correctly, the offset may also be a good indicator of TID damage over time resulting in possible radiation monitor applications for SOI detectors. Double SOI layers are currently being researched by the SOIPIX collaboration and may be a viable solution to the development of a monolithic SOI detector.

Along with more advanced TRAPPISTe chips, more sophisticated test systems will also need to be developed. The current test PCB provides the necessary biasing to the TRAPPISTe devices but lacks an integrated

high speed readout system. Currently, measurements are taken off board via coax connectors to an oscilloscope, resulting in high measurement parasitics. An integrated on board readout system would significantly reduce parasitics and better characterize the devices. The LARA test system can also be improved to reduce the uncertainty in laser positioning. A camera system could be installed to more accurately point the laser.

During the course of the TRAPPISTe project, both 3T and charge amplifier circuits have been developed. 3T circuits offer the advantages of compact size and low power performance. They rely on charge storage and subsequent readout using switches and pass gates. Charge amplifiers can provide real time charge information and advanced signal processing. However, they require more space and larger power consumption. One of the advantages of using SOI technology is the ability to incorporate advanced circuitry into a monolithic pixel. TRAPPISTe-2 has already shown that the integration of a basic amplifier is feasible. Future work can improve on the noise and power consumption of the amplifier and with the emergence of 3D integrated technology it may be possible to develop complete readout systems on a chip. The TRAPPISTe project can leverage these advantages to develop complete monolithic detector and readout systems.

TRAPPISTe-3 is foreseen to be designed in 2015 with new process techniques to prevent the backgate effect and to realize an improved monolithic detector in SOI technology.

APPENDIX A

Test Systems

As part of the TRAPPISTe project, a test PCB and a laser test system called LARA have been developed. These two systems were used to collect the test results presented in this thesis.

A.1 TRAPPISTe Test System

The TRAPPISTe test system was designed to provide the necessary biasing and readout for the TRAPPISTe-1 and TRAPPISTe-2 series of chips. To provide the flexibility of testing different chips, the system was divided into a main board and several daughter boards. The system is controlled by an Altera DE2 FPGA [111].

The main board provides the necessary bias voltages and currents for the test chips and an analog-to-digital (ADC) converter to read the signals from the test devices. Located on the main board are:

- DC voltage regulators providing 2.5V (for TRAPPISTe-1) and 3.3V and 1.8V (for TRAPPISTe-2)
- Two 8-bit DACs providing a total of 16 controllable voltage channels
- Seven voltage controlled current sources to provide bias currents
- A Maxim MAX1304 12-bit, 8 channel ADC to collect data from the test devices

The ADC and DACs on the main board are controlled by an Altera DE2 FPGA board. The FPGA board contains a Cyclone II FPGA running at 50MHz and provides programmable external inputs and outputs which can be configured for different test scenarios. The FPGA communicates by TCP/IP to a PC over Ethernet.

The main board accommodates a daughter board which holds the test device. The daughter boards provide the necessary socket adaptor to allow the TRAPPISTe PCB to interface with the various TRAPPISTe variants. A DB9 connector on each daughter board allows the connection of extra biasing voltages not provided by the main board. This includes voltages such as the back voltage used to bias the handle wafer. Three daughter boards have been produced:

- **Charge Amplifier Study Daughter Board**: The charge amplifier study daughter board holds a 48-pin DIP package. Several amplifiers were bonded into DIP packages at UCL's ICTEAM facilities.
- **TRAPPISTe-1 Daughter Board**: The TRAPPISTe-1 daughter board is designed to hold the TRAPPISTe-1 matrix. The chip is glued to a metal pad with a conductive adhesive and the wire bonds are made from the TRAPPISTe-1 bonding pads to the daughter board. During testing, the device needs to be covered to prevent stimulation from ambient light.

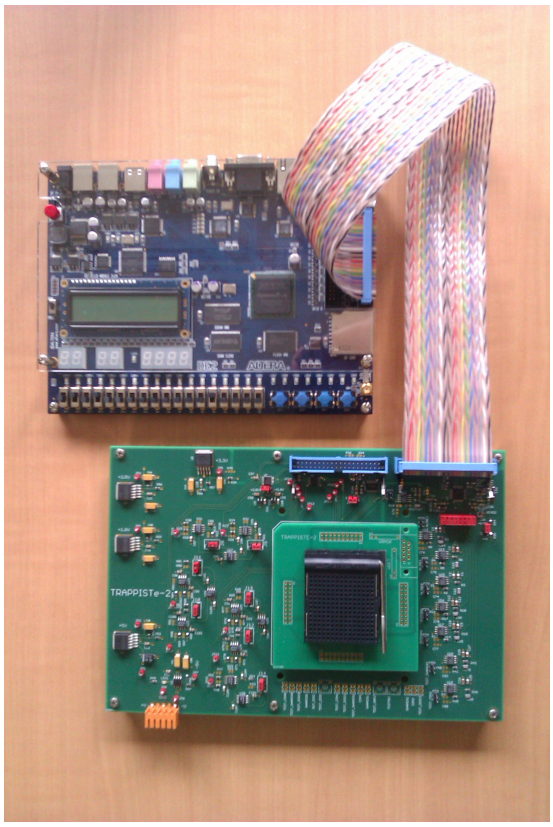

Figure A.1: TRAPPISTe PCB

- **TRAPPISTe-2 Daughter Board**: The TRAPPISTe-2 daughter board holds a 256-pin PGA socket. OKI provided several TRAPPISTe-2 devices already bonded into PGA packages.

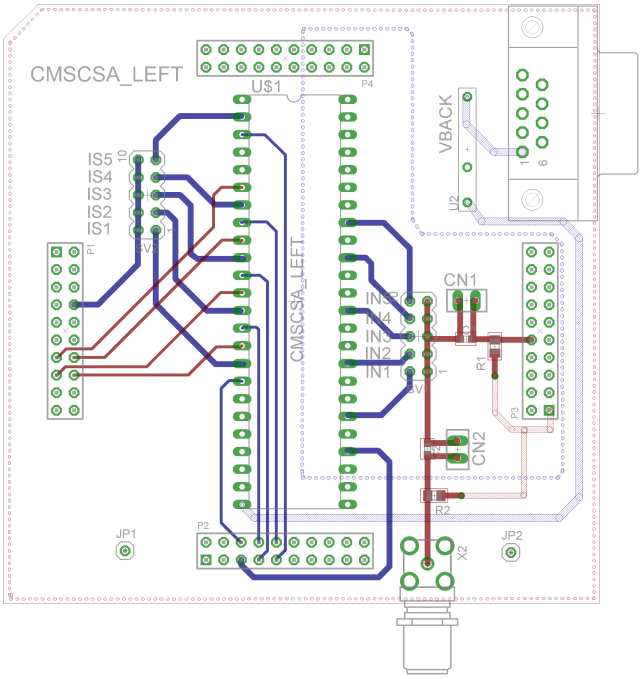

Figure A.2: Charge amplifier study daughter board

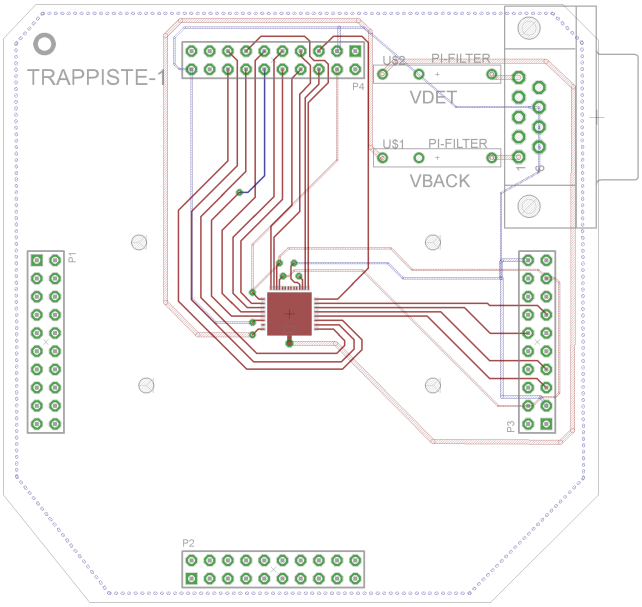

Figure A.3: TRAPPISTe-1 daughter board

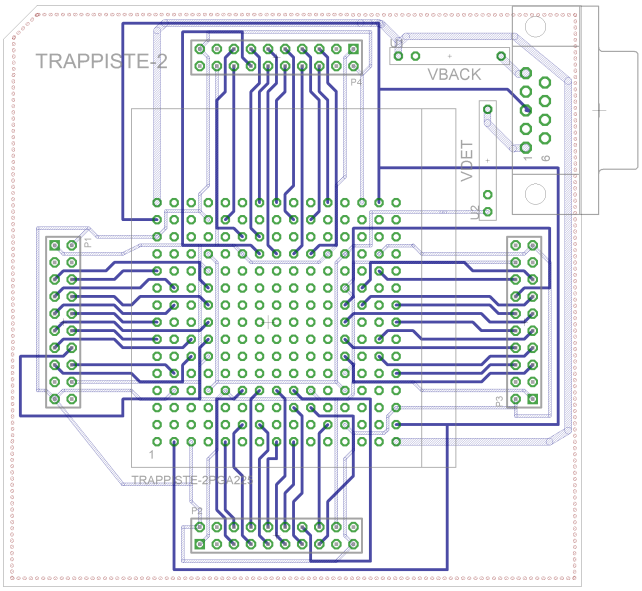

Figure A.4: TRAPPSITE-2 daughter board

A.2 LARA Laser System

A test system named Laser for Radiation Analysis (LARA) has been commissioned to allow the characterization of test devices with a laser. Laser systems can be used to create charge in semiconductor devices in order to study their charge collection behavior [112] [113], as described by the photon interaction mechanisms in Section 1.2.3. Two laser heads are available, an infrared laser at around 1060nm wavelength and a red laser at around 670nm wavelength.

Infrared lasers are often used in charge collection studies. The standard choice is an infrared laser around 1060nm wavelength. At this wavelength, the photon energy is about equal to the silicon bandgap energy of 1.1 eV. The infrared is at the edge of the silicon absorption spectrum, so that as the laser travels the silicon, part of it is absorbed creating electron-hole pairs and part of it continues through the sensor bulk. The created charges are collected at the biased electrodes of the detector (Figure A.5).

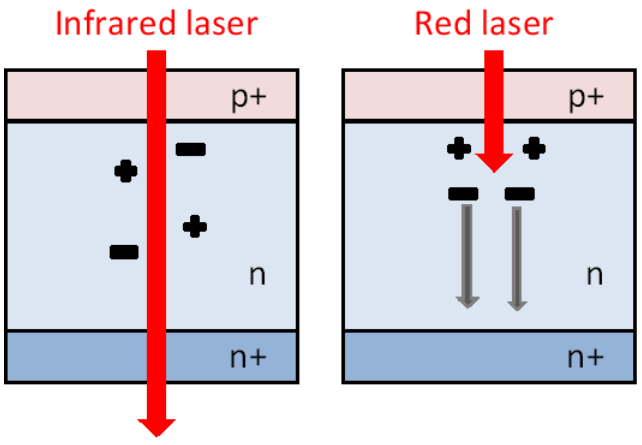

Figure A.5: An infrared laser traverses the whole detector, creating charges throughout the active area. A red laser penetrates only a few microns into the detector, creating charges near the surface which drift according to the electric field configuration.

Red lasers are used for the transient current technique. The transient current technique is a technique used to explore the electric field configuration in a detector. A red laser around 670nm wavelength is used as the excitation source. This wavelength corresponds to 1.9 eV of energy per photon, enough to cover the silicon bandgap and create electron-hole pairs. The red laser penetrates only a few microns in silicon so that charges are created closer to the entry side of the beam. For a p-on-n substrate detector, the holes created are quickly collected at the junction side electrode. However, the electrons will drift towards the other side of the detector (Figure A.5). This drift is affected by the potential field configuration in the detector and will be reflected in the pulse shape of the diode signal. A laser shone on the backside of the detector allows one to observe the electron drift.

A.2.1 LARA Setup

The LARA laser setup has a PicoQuant LDH 1060nm laser head controlled by a PicoQuant PDL 800-D controller. A three axis motorized stage is used to position a test device underneath the laser head. The stage is controlled remotely via computer and custom software can be coded in LabView.

A.2.2 Photon Calibration

The laser driver controls the intensity of the laser pulse delivered by the laser head. The intensity is controlled by a dial control which is labeled from 1 to 100. In order to determine how many photons are being emitted by the laser head for each intensity setting, the laser was calibrated with an UltraFast-20-SM photodiode by Advanced Laser Diode Systems.

The output of the laser was attached to the photodiode and the diode response was observed on an oscilloscope with the input impedance set to 50 ohms. The response of the diode is a fast voltage pulse on lasting on the order of 200 picoseconds. Figure A.7 shows an example measurement

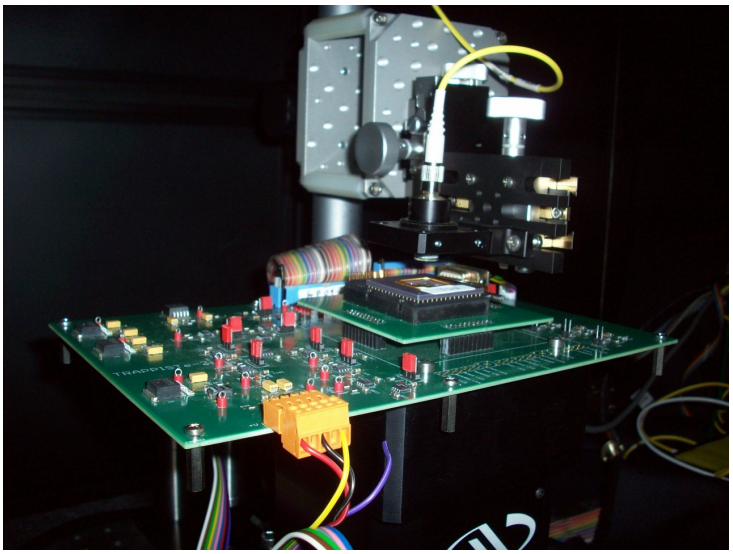

Figure A.6: LARA

with the intensity set at 20. The area of of the voltage pulse is recorded by the oscilloscope to give V·s. In this plot, the area of the curve is 4.79×10^{-11}V·s.

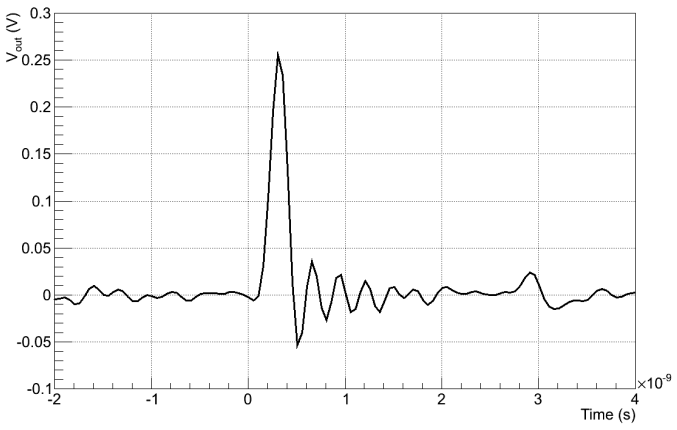

Figure A.7: UltraFast diode response to laser pulse of intensity setting 20.

This area is then converted to amperes·seconds by dividing by the 50 ohm impedance to give 9.58×10^{-13}A·s area. The efficiency of the diode is rated as 0.22 A/W meaning that the diode converts and incident energy of 1 W into 0.22A of current. Dividing the A·s area by 0.22 gives 4.35×10^{-12}W·s or joules of incident energy.

Assuming the amount of incident energy is equal to the energy emitted by the laser, the number of photons emitted by the laser be calculated by dividing by the emitted energy by the energy per photon. At 1060nm, the energy of a photon is 1.87×10^{-19}, resulting in 2.33×10^{7} photons being emitted per pulse at an intensity setting of 20. The same calculations were done at different intensities with the results shown in Figure A.8. All measurements were done at a laser pulse frequency of 50 Hz.

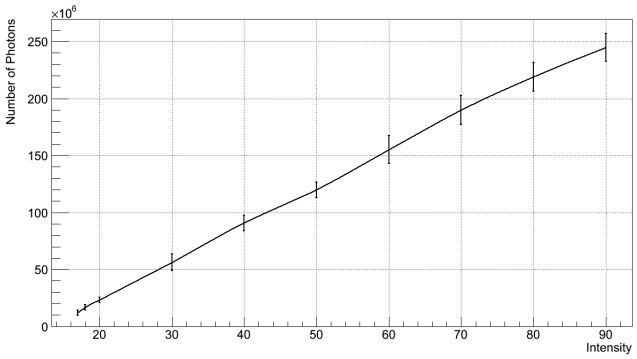

Figure A.8: Photons emitted per pulse vs laser intensity setting.

A.2.3 Beam Size Measurement

The approximate size of the LARA infrared beam was measured by Master's student Geoffrey Alexandre.

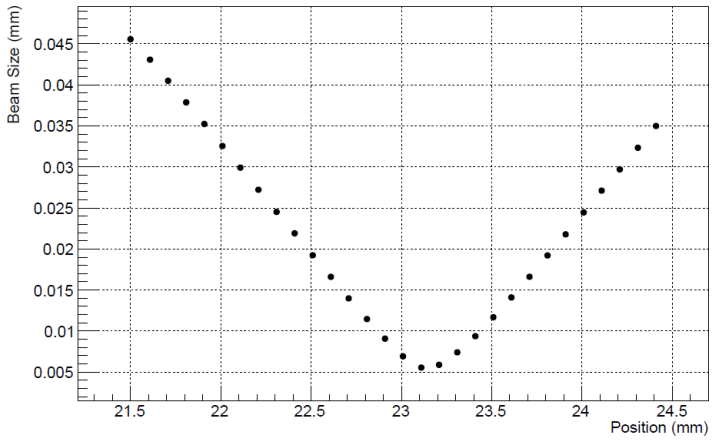

Figure A.9: LARA beam size measurement. Minimum spot size is $5\mu m$.

APPENDIX B

TRAPPISTe 3-Transistor Readout

This section describes the 3-Transistor structures implemented on TRAPPISTe-1 and TRAPPISTe-2.

B.1 TRAPPISTe-1 3T Readout

The TRAPPISTe-1 readout circuit is based on a standard 3-transistor (3T) architecture commonly used in active pixel sensors. This architecture can be implemented with a few transistors which is important when layout area is a concern, as is the case with TRAPPISTe-1. A basic 3T architecture is based on:

- a reset transistor that is used to set a potential at the floating detector node
- a buffer transistor that is connected to the detector node
- a selection transistor that is used to transmit the signal to the pixel output

Figure B.1 shows a schematic of the readout circuit implemented in each pixel of TRAPPISTe-1. Each transistor shown is an nMOS transistor. The reset transistor, M_{reset}, places a know reset voltage onto the detector node to remove any integrated charge. The reset transistor is controlled by a reset signal on the transistor gate. The buffer transistor, M_{buf1}, is a source follower that reads the voltage at the detector node without removing the charge on the detector. The buffer transistor is biased by the current source transistor $M_{source1}$. Instead of a selection transistor to transmit the signal, a switch has been implemented controlled by a Store signal. The charge information is stored onto a 59fF capacitor C_{store}. The value of the capacitor was determined by the size of capacitor that could be comfortably fit within the layout. The voltage on the capacitor is buffered by M_{buf2}, which is biased by the current source transistor $M_{source2}$. A second switch controlled by a Read signal is used to place the signal on the output pad. This pixel readout scheme allows for the charge information to be stored temporarily on the storage capacitor when the Store signal is activated and to be read out at a later time when the Read signal is activated.

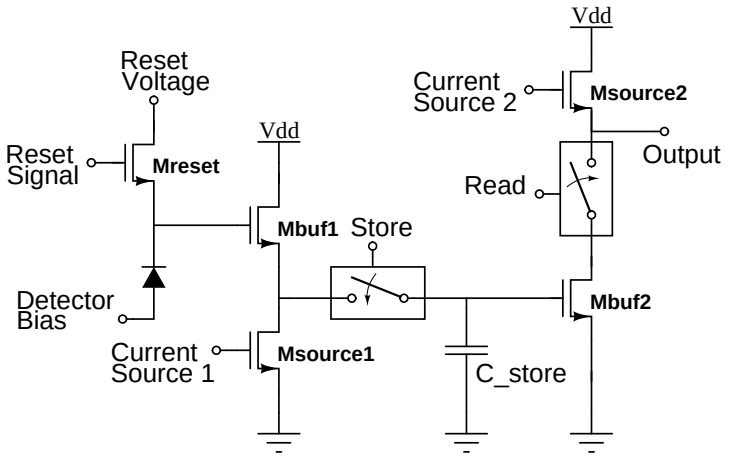

Figure B.1: Pixel readout circuit with storage capacitor and switches to control storage of the signal and reading of the signal at the output.

B.1.1 Shift Register

To control the readout of the pixel matrix, a shift register was created. The register consists of a series of eight D-latches controlled by a clock signal (see Figure B.2). The eight outputs of the D-latches are each connected to the Read signals of one column in the matrix. At the first rising edge clock signal, the first D-latch outputs a high signal which activates the Read signals in the first column. This places the signals in the first column pixels, which has been stored on the storage capacitor, on the row outputs. On the second rising edge of the clock, the second latch is outputs a high signal (while the first latch goes low) so that the second column of pixels is activated and placed on the row outputs. In this manner, the shift register activates each column in turn at each rising clock edge. The readout signals can be controlled by an external data acquisition system to give a continuous readout of the matrix by cycling through the eight columns.

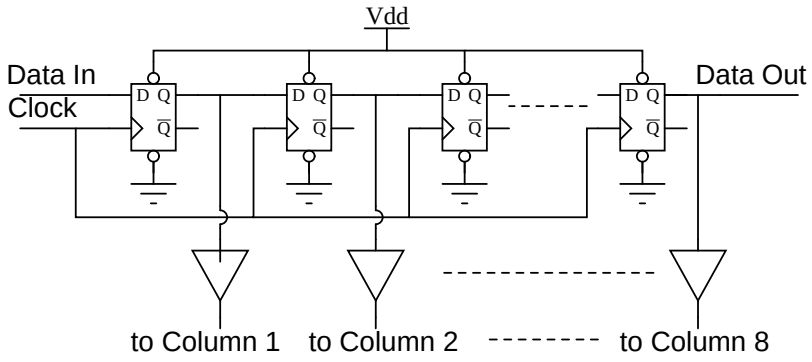

Figure B.2: Schematic of the shift register used to control column readout.

B.1.2 SPICE Simulation of Pixel Readout

Four versions of the readout circuit are implemented on TRAPPISTe-1 as shown in Figure 3.3. Each pixel contains a readout circuit with the same 3T architecture that is realized with one of four available transistor

types: standard V_t, high V_t, low V_t and graded channel. A given pixel contains only one type of transistor. Each readout circuit was simulated in ELDO SPICE, except for the graded channel readout as SPICE models for graded channel transistors were not available.

The DC gain and frequency response of the pixel cells are shown in Figures B.3 and B.4 respectively. The plots are taken from the Output node of the circuit (see Figure B.1). They show that the gain of the readout circuit is about -4 V/V, with an operating point around 1V for the low V_t pixels and 1.6V for the high and standard V_t pixels. The frequency response for all three types is similar, with a cutoff frequency around 470 kHz and a bandwidth around 1 MHz with a phase margin of 100 degrees.

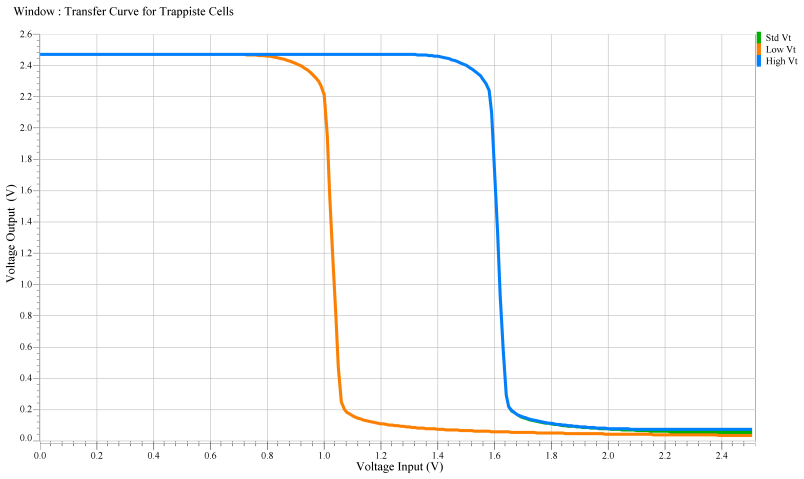

Figure B.3: Simulated transfer curves of the TRAPPISTe-1 readout circuit. Standard V_t and high V_t curves are almost identical with an operating point around 1.6V. The low V_t circuit has an operating point around 1V.

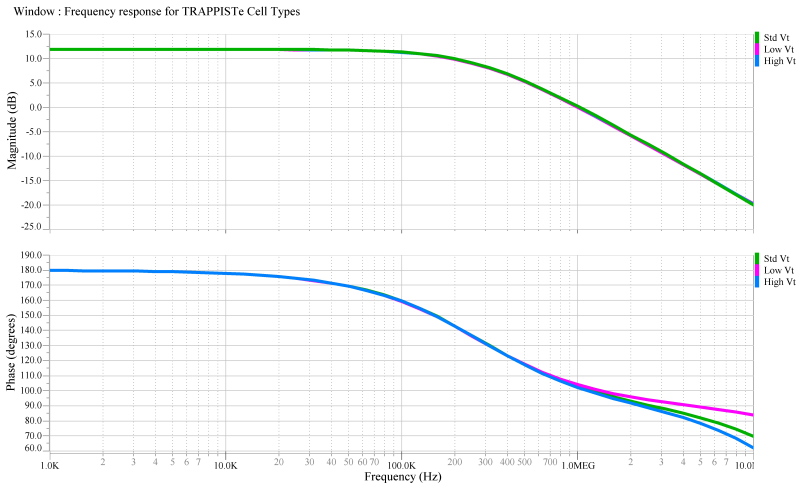

Figure B.4: Simulated frequency plot of the standard V_t, high V_t, low V_t variants of TRAPPISTe-1 readout circuit

B.2 TRAPPISTe-2 3T Readout

The 3T readout circuit of TRAPPISTe-2 is shown in Figure B.5. It is composed of Standard V_t transistors and it has the same architecture as that of TRAPPISTe-1. A reset transistor M1 is used to place a bias voltage ($V_{vnreset}$) onto the detector node which clears any charge accumulated on the detector. Transistor M3 buffers the signal and is biased by transistor M8. The selection transistor M4, controlled by the signal V_{nstore}, places the signal onto a 37.5fF storage capacitor C_{store}. When the signal on the storage capacitor is to be read out at the output, transistor M6 is opened via signal V_{nread}. The signal on the capacitor is buffered by transistor M5 which is biased by transistor M7.

As with TRAPPISTe-1, the 3T matrix on TRAPPISTe-2 is controlled by a shift register comprised of a series of D-latches. The shift register is located at the top of the matrix. Each of the three matrix rows has only one output pad, so that only one pixel in a given row can be output at a given time. The shift register is controlled by a clock signal that activates one column at a time on each clock pulse. When a column is

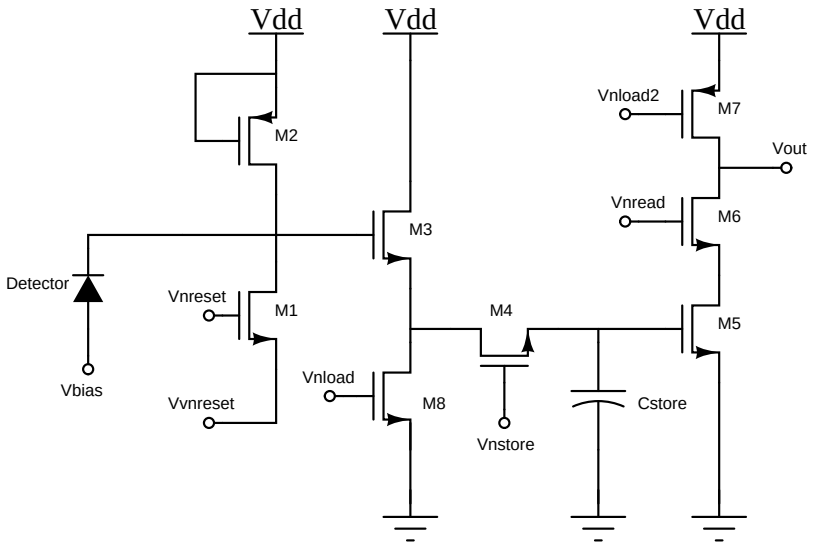

Figure B.5: 3T readout circuit for TRAPPISTe-2 pixel matrix.

activated, the read transistors M6 in each pixel throughout the column are activated so that the information in that column is placed on the output pads.

The first electrical characterizations of the 3T circuit have been made in August 2012. Sample measurements are shown in Figure B.6 indicating an operation point around 1.32V which are consistent up to a back voltage of 12V. Measurements have also been performed with a laser source indicating that the matrix is able to track the position of the source. These measurements have been presented at the SOIPIX 2012 conference [114] and will be continued to be studied within the TRAPPISTe project.

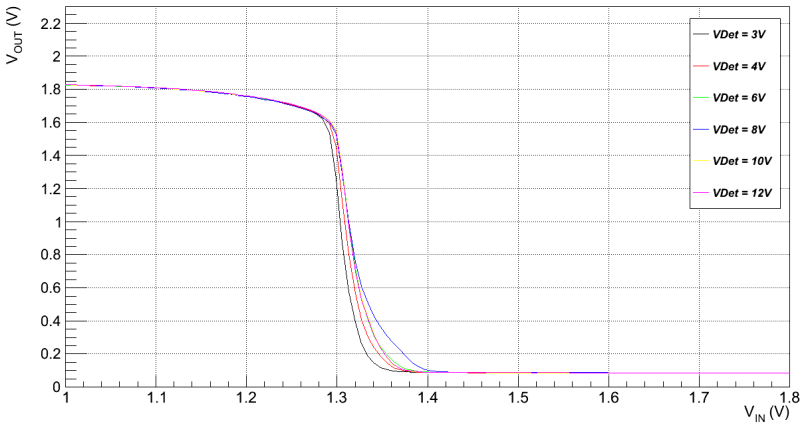

Figure B.6: Measured 3T transfer curves for TRAPPISTe-2 with different back voltage.

APPENDIX C

TRAPPISTe-2 Amplifiers Version 0 and Version 1

This section describes the test results of the version 0 and version 1 amplifiers.

C.1 CSA1 and CSA0 Measurements

After the tests on the CSA2 amplifier were performed, the other two versions of the charge sensitive amplifier, CSA1 and CSA0, were also characterized. These two versions of the amplifier were included in the layout in case the self-biased CSA2 amplifiers did not function correctly. As with the previous amplifier tests, the TRAPPISTe PCB provided the necessary biasing and results were recorded on a digital oscilloscope.

CSA1 is composed of low voltage transistors and CSA0 of standard voltage transistors. These two versions consist of the cascode core of the amplifier with direct biasing lines as shown in Figure C.1. M1 is the

input transistor with M3 the cascode transistor while M2 and M4 provide bias currents. The output can by adjusted by transistor M5 which is biased by transistor M6. Voltage biases VCSACTRL and VCSARF are applied directly to the shown bias points. Bias currents ICSAN, ICSAP and ICSALEVEL are provided via mirror transistors which are not shown.

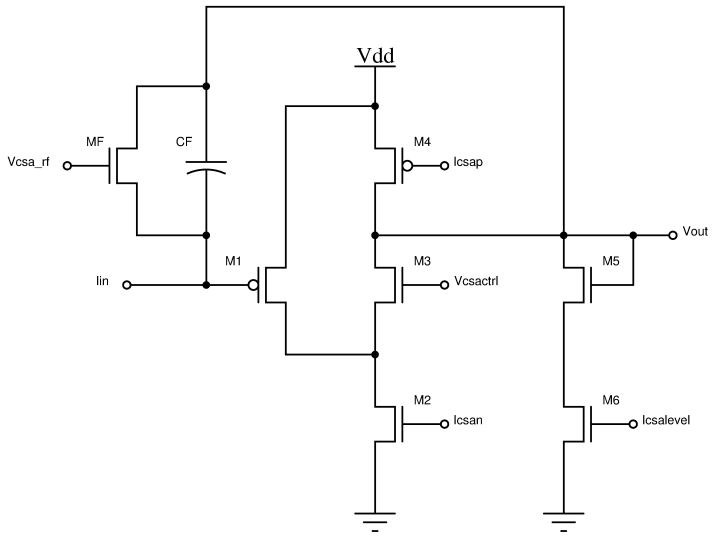

Figure C.1: CSA1 and CSA0 amplifier architecture with direct biasing. Voltages are applied directly. Current biases are applied via current mirrors (not shown in figure).

The determination of the amplifier bias points was achieved experimentally. Initial bias points based on simulation results were first applied to the test amplifiers; these values were then adjusted to obtain a measurable output signal. Table C.1 shows the final biasing values applied to CSA0 and CSA1 which were determined during experimental testing. The results shown in the chapter were obtained using these nominal bias values unless otherwise specified.

Bias	CSA1	CSA0
ICSAN	100 μA	140 μA
ICSAP	20 μA	30 μA
ICSALEVEL	2 μA	2 μA
VCSACTRL	1.2V	1.5V
VCSARF	1.0V	1.0V

Table C.1: Bias parameters for CSA1 and CSA0 testing.

Overall, the results of the CSA1 and CSA0 measurements show that the directly biased amplifiers exhibit similar behavior as the CSA2 amplifier. The following sections highlight the results of the CSA1 and CSA0 test structures.

C.1.1 CSA1 DC Measurements

The DC transfer curve of CSA1 was performed in the same manner as CSA2. An input voltage ramp from 0V to 1.8V was applied to the input and the resulting output was observed. It was not possible to perform DC tests on CSA0; due to the limited number of output pads on the outer IO ring the output of the DC test CSA0 could not be routed out. Figure C.2 shows a similar shift as seen in CSA2 in the DC curve as the back voltage increases. The operating point of the amplifier decreases from a nominal 0.9V to less than 0.4V with a back voltage of 11V. The DC gain decreases from -5V/V to less than -3.5V/V as plotted in Figure C.3. These results are comparable to the CSA2 results which also shows degradation in the amplifier performance as the back voltage is increased. At around 12V of applied back voltage the amplifier can no longer function properly.

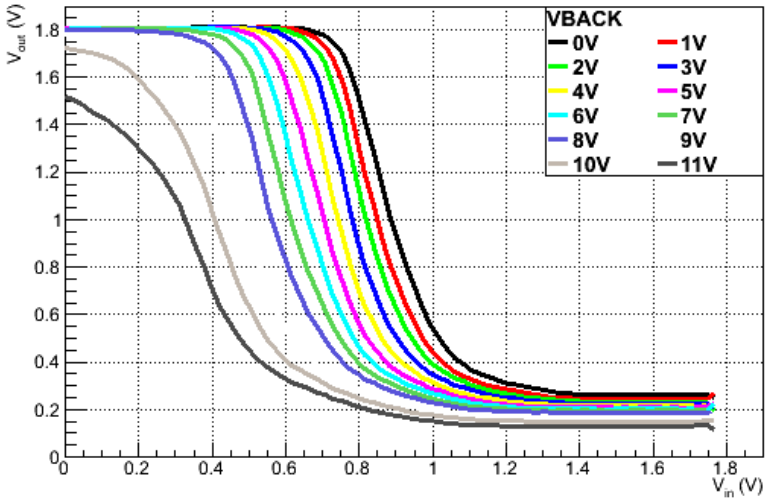

Figure C.2: Shift of CSA1 DC response with varying back bias voltage.

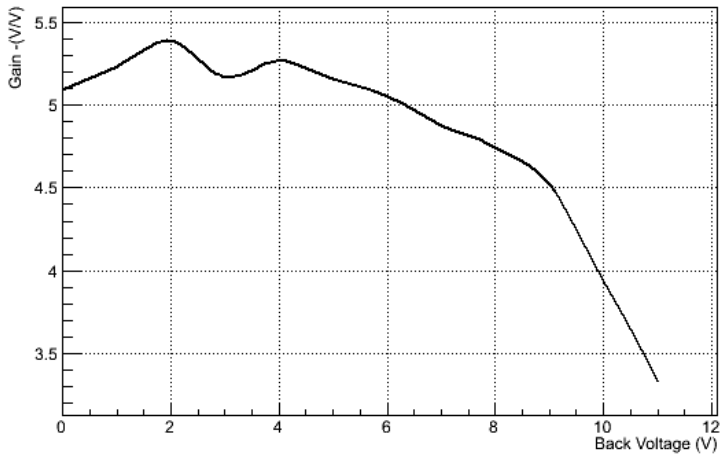

Figure C.3: Reduction in DC gain for CSA1 with increasing back voltage.

C.1.2 CSA1 and CSA0 Transient Measurements

Transient measurements were performed on the CSA0 and CSA1 test structures with the output recorded on an oscilloscope. As with CSA2, an on-chip 37.5fF series was implemented in the circuit layout at the amplifier input. Charge was injected by applying a voltage pulse on the capacitor with a square wave generator. Figures C.4 and C.5 show the response of the CSA1 and CSA0 respectively to an input of around 23,000 electrons, equivalent to 1 MIP in 300 μm of silicon. Both amplifiers show similar outputs; CSA1 has a max amplitude response of 64mV and CSA0 has a slightly lower response of 56mV. The strong sensitivity to the feedback voltage V_{RF} is also present, with the risetime rapidly decreasing from greater than 160μs to 5μs within a VRF range of 0.9V to 1.3V.

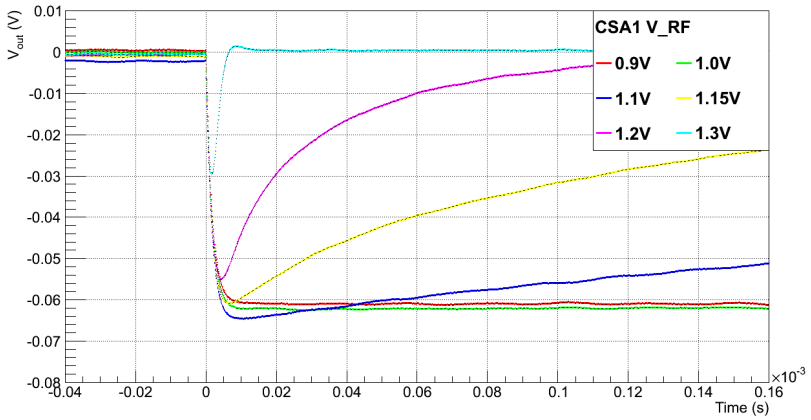

Figure C.4: CSA1 transient response with varying feedback transistor voltage.

C.1.3 CSA1 and CSA0 Response to Back Voltage

The response of CSA1 and CSA0 to an applied back voltage is shown in Figures C.6 and C.7. As with CSA2, there is a marked decrease in

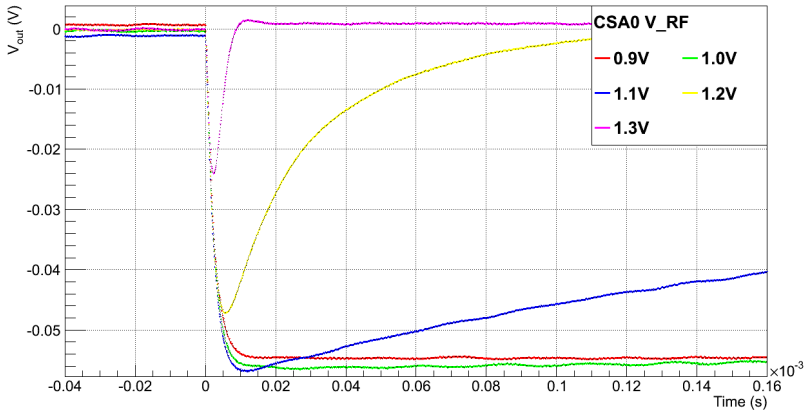

Figure C.5: CSA0 transient response with varying feedback transistor voltage.

signal amplitude and signal risetime as the back voltage is increased. CSA0 fairs slightly better than CSA1 in response to the back voltage; at VBACK=7V, the amplitude of CSA1 has decreased by half whereas the amplitude for CSA0 has decreased by one third. This can be a result of the CSA0 amplifier operating at a higher operating point due to the higher voltage threshold transistors. This gives the amplifier operating point more margin to decrease as the the back voltage is increased.

C.2 Shaper1 and Shaper0 Transient Measurements

Shaper1 and Shaper0 contain the same core amplifier as Shaper2 except with direct biasing instead of biasing transistors. The have the same value series input capacitor (200fF) and the same value feedback capacitor (50fF) as Shaper2. Shaper1 is composed of low voltage transistors and Shaper0 is comprised of standard voltage transistors. The voltage and current bias points are shown in Figure C.8. Voltage biases are ap-

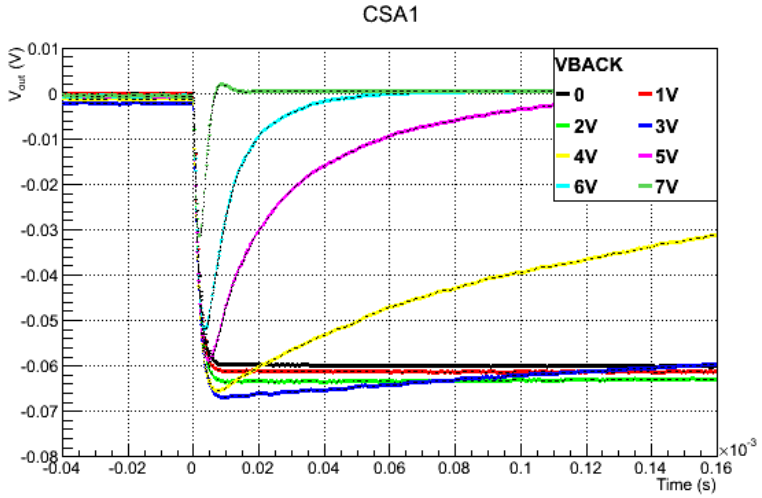

Figure C.6: CSA1 transient response with varying back voltage.

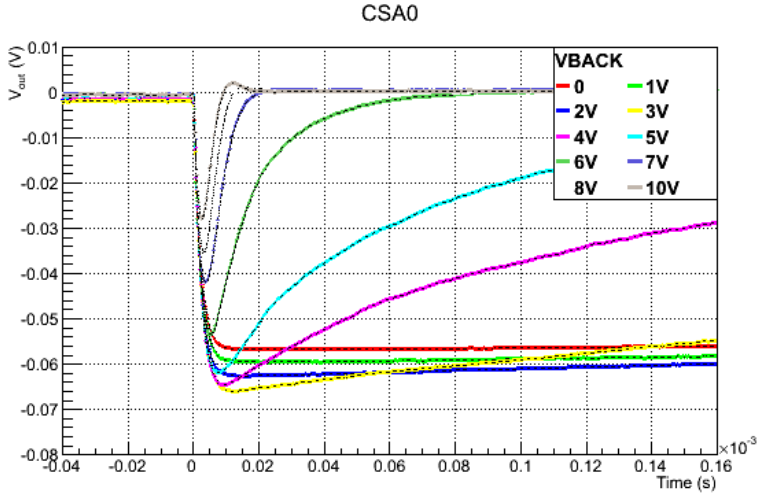

Figure C.7: CSA0 transient response with varying back voltage.

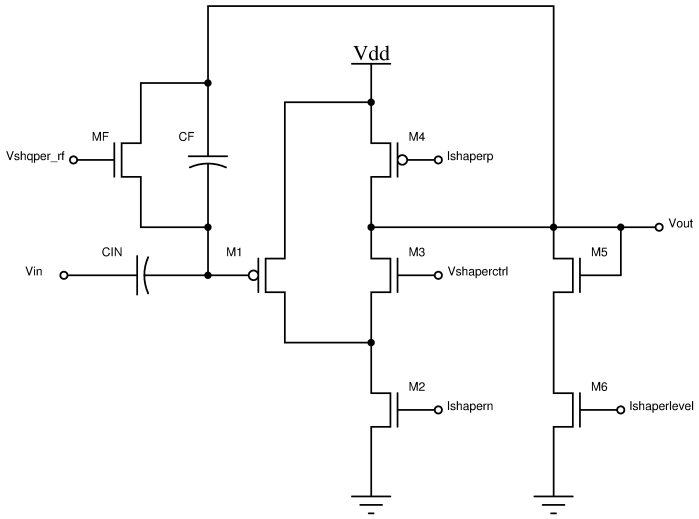

Figure C.8: Schematic of SHAPER0 and SHAPER1 showing bias points. Bias voltages are applied directly. Bias currents are provided via mirror transistors (not shown in figure).

plied directly and currents are applied via mirror transistors which are not shown.

The bias points were determined experimentally. Initial values determined from SPICE simulations were set and then modified during testing to obtain a good measurable output response. Table C.2 shows the bias values used for the shaper amplifiers. These values are identical for both shapers, except for the feedback transistor voltage which is slightly higher for Shaper0 (1.1V) than for Shaper1(1.0V). These values were used for all transient measurements unless otherwise specified.

Shaper1 and Shaper0 were characterized with the same experimental setup as Shaper2. A charge input was applied to the CSA-Shaper amplifier chain via an on-chip 37fF series capacitor and the output was recorded on an oscilloscope. The shaper response for these two versions

Bias	Shaper1	Shaper0
ISHAPERN	30 μA	30 μA
ISHAPERP	10 μA	10 μA
ISHAPERLEVEL	1 μA	1 μA
VSHAPERCTRL	1.5V	1.5V
VSHAPERRF	1.2V	121V

Table C.2: Bias parameters for Shaper1 and Shaper0 testing.

was similar to that of Shaper2 and some example plots are shown in this section.

Figures C.9 and C.10 show the response of Shaper1 and Shaper0 to a charge injection of 23,000 electrons at the CSA-Shaper chain input. As noticed during the testing of Shaper2, the parasitic capacitances of the test setup results in large shaping times. The shaping time of the signal can be controlled by the voltage on the feedback transistor VSHAPERRF. As the shaping time is decreased, the signal is attenuated as the signal risetime is not sufficient to reach the maximum amplitude.

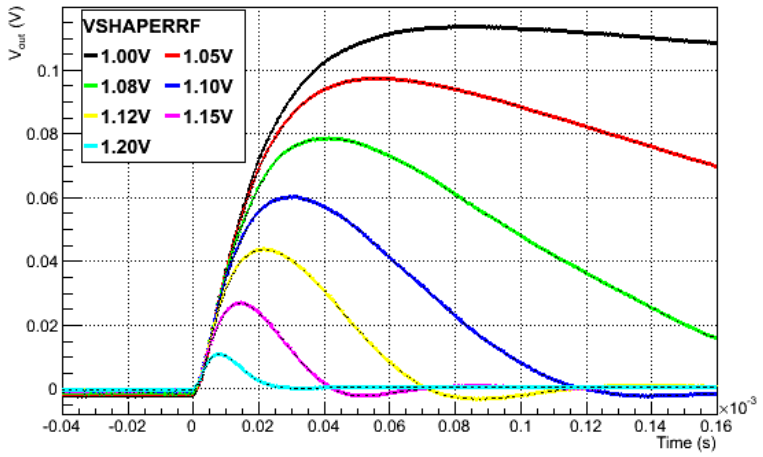

Figure C.10: Shaper0 transient response to input charge of 23,000 electrons with different feedback transistor voltage.

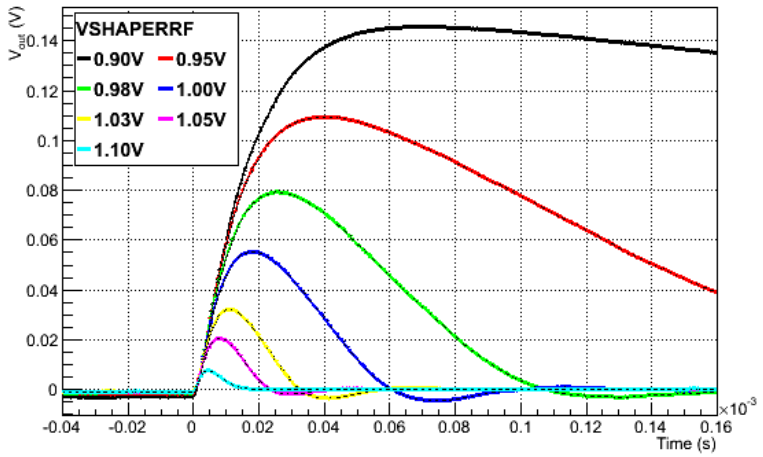

Figure C.9: Shaper1 transient response to input charge of 23,000 electrons with different feedback transistor voltage.

The response to an applied back voltage for Shaper1 and Shaper0 is shown in Figures C.11 and C.12. The input charge for these measure-

ments is around 23,000 electrons. As with Shaper2, the shaper amplitude diminishes strongly with varying back voltage VBACK, dropping to one third of the initial value at 2V. In a monolithic detector system, the back voltage would be used to deplete the sensor in the handle wafer. These results indicate that only a low back voltage can be applied or else the output signal would be too attenuated.

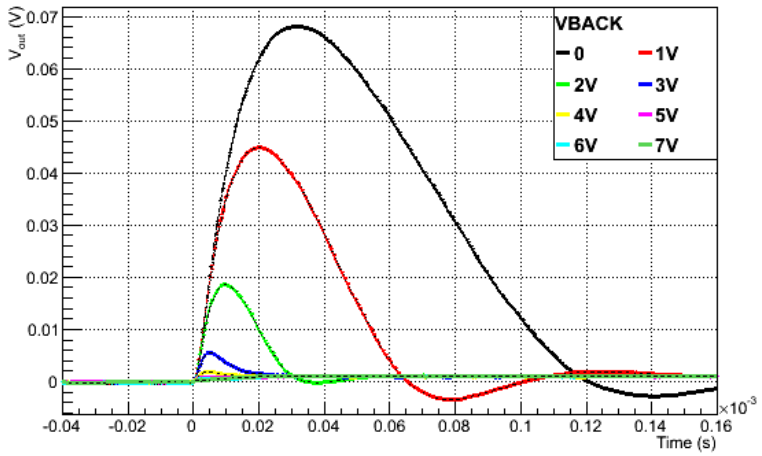

Figure C.11: Shaper1 transient response to input charge of 23,000 electrons with varying back voltage.

C.3 CSA1 and CSA0 Pixel Measurements

As with the CSA2 amplifier matrix, the same laser measurements were performed on the CSA1 and CSA0 amplifiers in the sixth pixel column. As with the standalone test structures, the CSA1 and CSA0 amplifiers contain the same core architecture as CSA2 but require more biasing. The same trends in operation were observed as with the CSA2 amplifier and a few example measurements are shown here. The transient measurements in Figures C.13 and C.14 show the signal response to an

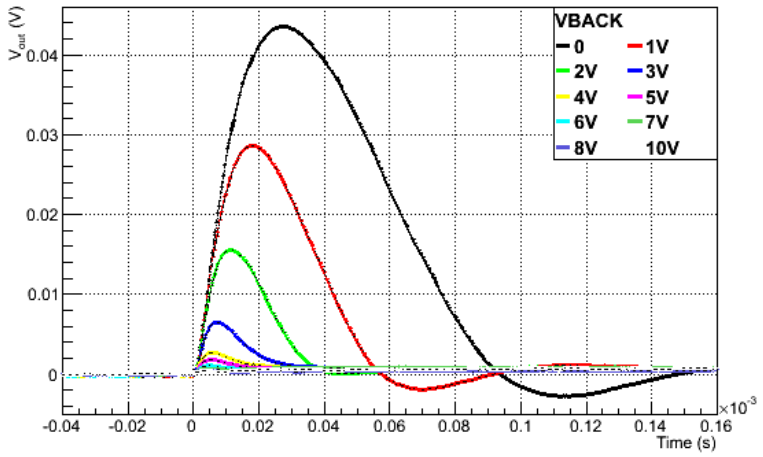

Figure C.12: Shaper0 transient response to input charge of 23,000 electrons with varying back voltage.

incident laser intensity of around 50x10^6 photons. The CSA0 amplifier has a slightly lower signal response which is consistent with the standalone test amplifier results in Chapter 4.

Figures C.15 and C.16 show the evolution of the signal amplitude with regards to V_{back} . As the V_{back} voltage initially increases, the amplifier output increases as the depletion width increases and more charge is collected. This continues until about 5V when the backgate effect causes the amplifier to no longer amplify correctly.

C.4 Shaper1 and Shaper0 Pixel Measurements

Shaper1 in the second row and Shaper0 in the first row were also characterized in the same manner as Shaper2. The 1060nm laser intensity was set to 50x10^6 and the frequency of the pulses set to 50Hz. As expected,

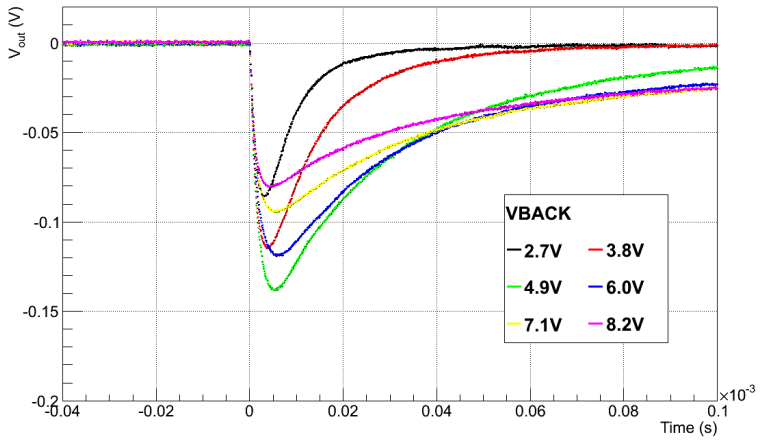

Figure C.13: CSA1 transient response to the 1060nm laser with varying V_{back}.

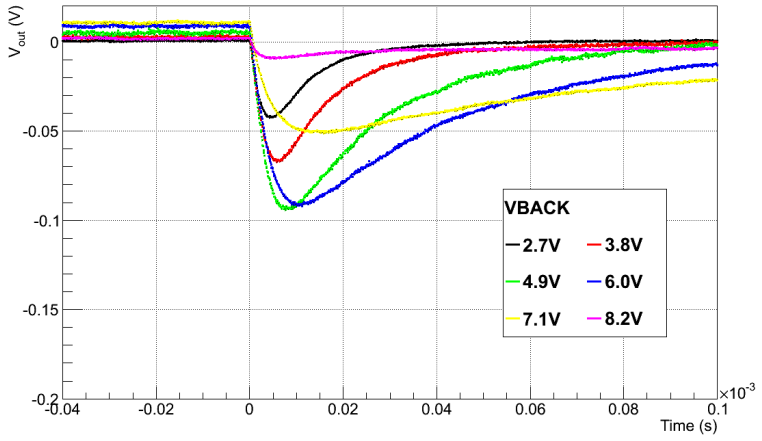

Figure C.14: CSA0 transient response to the 1060nm laser with varying V_{back}.

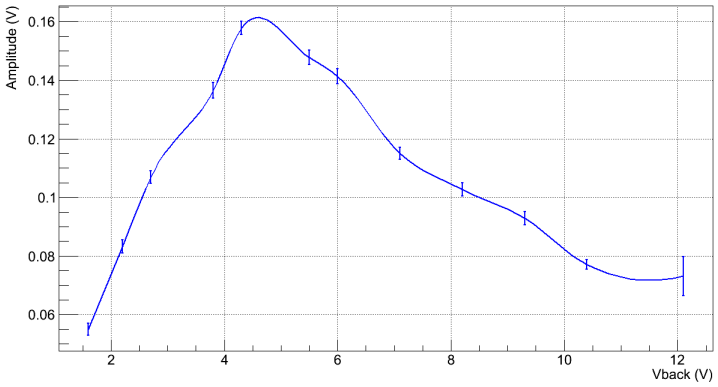

Figure C.15: CSA1 peak-to-peak amplitude response to the 1060nm laser with varying Vback.

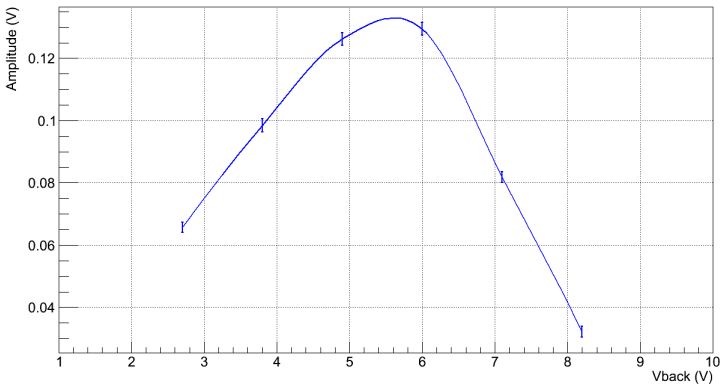

Figure C.16: CSA0 peak-to-peak amplitude response to the 1060nm laser with varying Vback.

the output of the shaper followed the same trend as the output of the CSA amplifiers. Figures C.17 and C.18 show the peak-to-peak amplitude of the transient signal at various value for V_{back}. As with the previous measurements, the signal amplitude increases with increasing depletion width until a V_{back} of 5V after which the backgate effect dominates and the signal amplitude decreases.

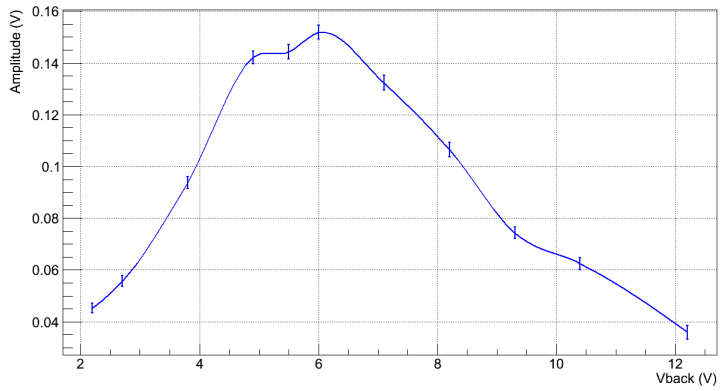

Figure C.17: Peak-to-peak amplitude response of Shaper1 to the 1060nm laser with varying V_{back}.

Pixel Targeting

The pixels with integrated amplifiers Shaper1 in the second row and Shaper0 in the first row were also tested for laser tracking. The laser was positioned over the pixel in the third column and the shaper output of every pixel in the row was recorded on the oscilloscope. Figures C.19 and C.20 show the outputs of Shaper1 and Shaper0 respectively. The output of the targeted pixel 3 for the Shaper1 row is around three times higher than the other pixels. This result is consistent with Shaper2 measurements which is not surprising as they are both contain the same core architecture with low voltage transistors.

However, Shaper0, which is constructed of standard voltage transistors, exhibits less desirable results. The lower output voltage of the Shaper0

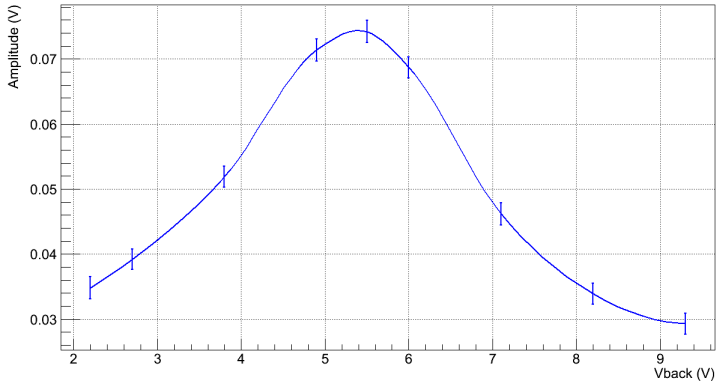

Figure C.18: Peak-to-peak amplitude response of Shaper0 to the 1060nm laser with varying V_{back}.

amplifier makes it more difficult to distinguish from neighboring pixels. The targeted pixel 3 output (0.14V) is less than 50% higher than neighboring pixel 4 (0.11V). Even the output pixel 1 (0.55V) which is two pixels away is 40% of the target pixel output. This makes it more difficult to determine the position of the incident radiation. The spread of the signal may be explained by the uncertainty of the laser position within the pixel and the spread of the laser beam size as discussed earlier in Section 5.3.1. However, given the same experiment conditions, Shaper2 and Shaper1 appear to perform better than Shaper0 in the integrated pixel matrix.

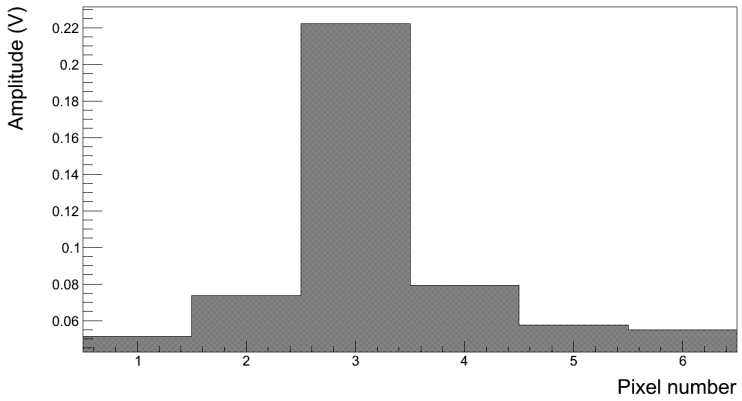

Figure C.19: Pixel response of Shaper1 with laser centered on pixel in column 3.

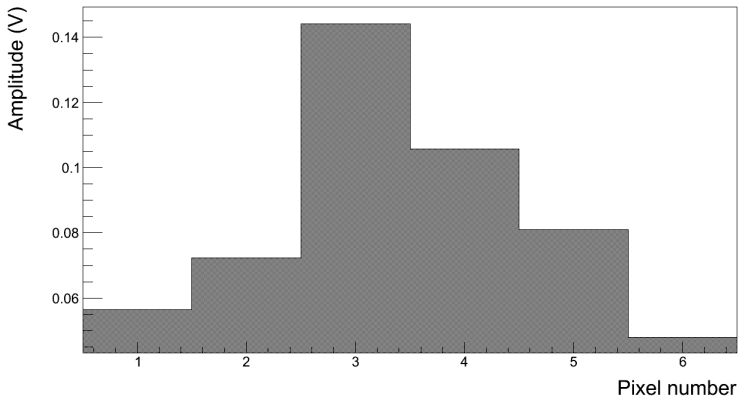

Figure C.20: Pixel response of Shaper0 with laser centered on pixel in column 3.

References

[1] O. Bruning *et al.*, "LHC Luminosity and Energy Upgrade: A Feasibility Study," European Organization for Nuclear Research, Tech. Rep. LHC Project Report 626, 2002.

[2] J. Brau, Y. Okada, and N. Walker, "International Linear Collider: Reference Design Report," International Linear Collider, Tech. Rep. Volume 1: Executive Summary, 2007.

[3] P. Lebrun *et al.*, "The CLIC Programme," European Organization for Nuclear Research, Tech. Rep. CERN-2012-005, 2012.

[4] L. Rossi, T. Rohe, P. Fischer, and N. Wermes, *Pixel Detectors: From Fundamentals to Applications*. Springer, 2006.

[5] Y. Allkofer *et al.*, "Design and performance of the silicon sensors for the CMS barrel pixel detector," *Nucl. Instr. and Meth. in Phys. Research*, vol. A 584, pp. 25–41, 2008.

[6] Wallonia Infrastructure Nano FABrication - WINFAB. [Online]. Available: http://www.uclouvain.be/winfab.html

[7] L. Soung Yee, E. Martin, E. Cortina, C. Renaux, and D. Flandre, "TRAPPISTe-1 Monolithic Pixel Detector in SOI Techonology,"

2010, Poster Presentation at the 2010 Vienna Conference on Instrumentation. [Online]. Available: http://indico.cern.ch/contributionDisplay.py?contribId=167&confId=51276

[8] ——, "Charge sensitive amplifier study in 2um FD SOI CMOS," in *Proceedings of the 2011 IEEE International SOI Conference (SOI)*, 2011. [Online]. Available: http://dx.doi.org/10.1109/SOI.2011.6081694

[9] L. Soung Yee, P. Alvarez, E. Martin, E. Cortina, and C. Ferrer, "Test of the TRAPPISTe Monolithic Detector System," in *Proceedings of the PIXEL 2012*, 2012. [Online]. Available: http://dx.doi.org/10.1016/j.nima.2013.03.052

[10] ——, "A Monolithic Pixel Sensor (TRAPPISTe-2) for Particle Physics Instrumentation in OKI $0.2\mu m$ SOI Technology," in *Proceedings of the TWEPP 2012*, 2012. [Online]. Available: http://dx.doi.org/10.1088/1748-0221/7/12/C12028

[11] (2007) Bandgap. [Online]. Available: http://en.wikipedia.org/wiki/File:Isolator-metal.svg

[12] G. Lutz, *Semiconductor Radiation Detectors*. Berlin: Springer, 1999.

[13] (2010) Pn-junction image. [Online]. Available: http://commons.wikimedia.org/wiki/File:Pn-junction-equilibrium-graph.svg

[14] J. Beringer and others (Particle Data Group), "2012 Review of Particle Physics," *Physical Review D*, vol. 86, no. 010001, 2012.

[15] (2010) Particle Data Group: Atomic Nuclear Properties. [Online]. Available: http://pdg.lbl.gov/2012/AtomicNuclearProperties/HTML_PAGES/014.html

[16] (1998) ARIES program. [Online]. Available: http://www-ferp.ucsd.edu/LIB/PROPS/PHOTON/

[17] (2012) Photovoltaic Education Network: Optical Properties of Silicon. [Online]. Available: http://www.pveducation.org/pvcdrom/appendicies/optical-properties-of-silicon

[18] H. Spieler, *Semiconductor Detector Systems.* Oxford, Great Britain: Oxford University Press, 2008.

[19] (2012) Synopsis TCAD. [Online]. Available: http://www.synopsys.com/tools/tcad/Pages/default.aspx

[20] Weightfield2. [Online]. Available: http://personalpages.to.infn.it/~cartigli/Weightfield2/Main.html

[21] M. Moll, "Radiation tolerant semiconductor sensors for tracking detectors," *Nucl. Instr. and Meth. in Phys. Research*, vol. 565, pp. 202–211, 2006.

[22] Z. Li, "Radiation damage effects in Si materials and detectors and rad-hard Si detectors for SLHC," in *PIXEL 2008 International Workshop*, 2009.

[23] M. Moll, "Development of radiation hard sensors for very high luminosity colliders - cern-rd50 project," *Nucl. Instr. and Meth. in Phys. Research*, vol. 530, pp. 1–6, 2004.

[24] M. Dentan, "Radiation Effects on Electronic Components and Ciruits," 2000, CERN Training Course Notes.

[25] N. Goddard Space Flight Center, "Single Event Effect Criticality Analysis," NASA, Tech. Rep. 431-REF-000273, 1996.

[26] G. F. Knoll, *Radiation Detection and Measurement*, 3rd ed. John Wiley & Sons, Inc., 2000.

[27] B. Hyams, U. Koetz *et al.*, "A silicon counter telescope to study short-lived particles in high-energy hadronic interactions," *Nucl. Instr. and Meth. in Phys. Research*, vol. 205, pp. 99–105, 1983.

[28] C. Hill *et al.*, "Operational experience and performance of the cdfii silicon detector," *Nucl. Instr. and Meth. in Phys. Research*, vol. 511, pp. 97–105, 2003.

[29] D. Collaboration, "D0 Run 2B Silicon Detector Upgrade Technical Design Report," Tech. Rep. Fermilab-Proposal-0925, 2001.

[30] D. Acosta *et al.*, "The CMS Physics Technical Design Report Voume 1: Detector Performance and Software," CMS Collaboration, Tech. Rep. CERN/LHCC 2006-001, 2006.

[31] A. Collaboration, "The ATLAS Detector and Physics Performance: Technical Design Report Voume," Tech. Rep. CERN/LHCC 99-14, 1999.

[32] M. Caolino *et al.*, "Two years of flight of the pamela experiment: results and perspectives," in *Proceedings of the International Workshop on Advances in Cosmic Ray Science*, no. arXiv:0810.480, 2008.

[33] A. Collaboration, "The alpha magnetic spectrometer (ams) on the international space station: Part i results from the test flight on the space shuttle," *Physics Reports*, vol. 366, pp. 331–405, 2002.

[34] ——, "First result from the alpha magnetic spectrometer on the international space station: Precision measurement of the positron fraction in primary cosmic rays of 0.5 to 350 gev," *Physical Review Letters*, vol. 110, no. 141102, 2013.

[35] G. Hall and P. Sharp, "CMS installs the world's largest silicon detector," *CERN Courrier*, February 1983. [Online]. Available: http://cerncourier.com/cws/article/cern/32915

[36] R. D. on behalf of the CMS Tracker, "Recent Results for the CMS Tracker Silicon Detectors," *IEEE Trans. Nucl. Sci.*, vol. 48, pp. 2299–2302, 2001.

[37] R. Castaldi, P. Siegrist, J.-E. Augustin, M. D. Negra, and E. Radermacher, "The Tracker Project Technical Design Report," CMS Collaboration, CMS TDR 5 CERN/LHCC 98-6, 1998.

[38] J. Kemmer, "Fabrication of low noise silicon radiation detectors by the planar process," *Nucl. Instr. and Meth. in Phys. Research*, vol. 169, pp. 499–502, 1980.

[39] E. Belau, R. Klanner *et al.*, "Charge collection in silicon strip detectors," *Nucl. Instr. and Meth. in Phys. Research*, vol. 214, pp. 253–260, 1983.

[40] N. Bachetta *et al.*, "The CMS silicon microstrip detectors: research and development," *Nucl. Instr. and Meth. in Phys. Research*, vol. 426, pp. 16–23, 1999.

[41] P. Holl *et al.*, "A double-sided silicon strip detector with capacitive readout and a new method of integrated bias coupling," *IEEE Trans. Nucl. Sci.*, vol. 36, no. 1, pp. 251–255, 1989.

[42] M. Planck Institut, "The MPI Halbleiterlabor Research Activities," 2007, brochure.

[43] R. Bailey, C. J. S. Damerell *et al.*, "First Measurements of Efficiency and Precision of CCD Detectors for High Energy Physics," *Nucl. Instr. and Meth. in Phys. Research*, vol. 213, pp. 201–215, 1983.

[44] C. J. S. Damerell, R. L. English *et al.*, "A CCD based vertex detector for SLD," *Nucl. Instr. and Meth. in Phys. Research*, vol. 288, pp. 236–239, 1990.

[45] Z. Zhang *et al.*, "Charge shielding in the In-situ Storage Image Sensor for a vertex detector at the ILC," *Nucl. Instr. and Meth. in Phys. Research*, vol. 607, pp. 538–543, 2009.

[46] S. Albergo, A. Alberigi, and E. H. M. Heijne, "RD19 : status report on activities in 1996-1997. Development of hybrid and monolithic semiconductor micropattern pixel detectors," CERN, Tech. Rep. CERN-LHCC-97-059, 1997.

[47] K. H. Becks *et al.*, "Commissioning of the DELPHI pixel detector," *Nucl. Instr. and Meth. in Phys. Research*, vol. 418, no. 1, pp. 15–21, November 1998.

[48] A. B. for the CMS Collaboration, "The CMS pixel detector and challenges (prospectives) for its upgrade," *Nucl. Instr. and Meth. in Phys. Research*, vol. A 624, no. 2, pp. 286–389, 2010.

[49] A. Dorokhov *et al.*, "High resistivity CMOS pixel sensors and their application to the STAR PXL detector," *Nucl. Instr. and Meth. in Phys. Research*, vol. 650, pp. 174–177, 2011.

[50] (2008) Wire bonding image. [Online]. Available: http://en.wikipedia.org/wiki/File:Wirebonding2.svg

[51] (2008) Flip chip image. [Online]. Available: http://en.wikipedia.org/wiki/File:Flip_chip_mount_1.svg

[52] J. Kemmer and G. Lutz, "New detector concepts," *Nucl. Instr. and Meth. in Phys. Research*, vol. 253, no. 3, pp. 365–377, 1987.

[53] J. Kemmer, G. Lutz *et al.*, "Experimental confirmation of a new semiconductor detector principle," *Nucl. Instr. and Meth. in Phys. Research*, vol. 288, no. 1, pp. 92–98, 1990.

[54] S. Rummel and L. Andricek, "The DEPFET active pixel sensor for vertexing at ILC and SuperKEKB," *Nucl. Instr. and Meth. in Phys. Research*, vol. 623, pp. 189–191, 2010.

[55] R. H. Richter *et al.*, "Design and technology of DEPFET pixel sensors for linear collider applications," *Nucl. Instr. and Meth. in Phys. Research*, vol. 511, pp. 250–256, 2003.

[56] R. Turchetta *et al.*, "A monolithic active pixel sensor for charged particle tracking and imaging using standard VLSI CMOS technology," *Nucl. Instr. and Meth. in Phys. Research*, vol. 458, pp. 677–689, 2001.

[57] I. Peric, "Active pixel sensors in high-voltage CMOS technologies for ATLAS," *Journal of Instrumentation*, vol. 7, 2012. [Online]. Available: http://doi:10.1088/1748-0221/7/08/C08002

[58] G. Deptuch *et al.*, "3d technologies for large area trackers," in *Proceedings of Snowmass 13*, no. arXiv:1307.4301v1, 2013.

[59] R. Lipton, "3d detector/electronics integration technologies - applications to LC, SLHC and photon sources," 2010, Poster Presentation at the 2010 SLAC Instrumentation Seminar.

[60] J. E. Lilienfeld, "Method and apparatus for controlling electric current," U.S. Patent 1 745 175, October 8, 1930.

[61] (2012) SOITEC Website. [Online]. Available: http://www.soitec.com

[62] (2007) Smart Cut process image. [Online]. Available: http://en.wikipedia.org/wiki/File:Smart_Cut_SOI_Wafer_Manufacturing_Schema.svg

[63] J. R. Schwank *et al.*, "Radiation Effects in SOI Technologies," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, pp. 522–538, 2003.

[64] J. P. Colinge, *Silicon-On-Insulator Technology: Materials to VLSI*, 3rd ed. Springer, 2004.

[65] O. Kononchuk, G. Riou, R. Brun, and C. Moulin, "Metrology Challenges for the Ultra-thin SOI," in *Proceedings of Frontiers of Characterization and Metrology for Nanoelectronics: 2011*, 2011, pp. 183–187. [Online]. Available: http://link.aip.org/link/doi/10.1063/1.3657887

[66] J. P. Colinge, "What is SOI?" 2009, presentation. [Online]. Available: http://www.eurosoi.org/tutorials.asp

[67] B. Diebrickx *et al.*, "Integration of CMOS-electronics and particle detector diodes in high-resistivity silicon-on-insulator wafers," *IEEE Trans. Nucl. Sci.*, vol. 40, no. 4, pp. 753–758, August 1993.

[68] J. Marczewski *et al.*, "Technology development for SOI monolithic pixel detectors," *Nucl. Instr. and Meth. in Phys. Research*, vol. 560, pp. 26–30, 2006.

[69] (2012) KEK - High Energy Accelerator Research Organization. [Online]. Available: http://legacy.kek.jp/intra-e/

[70] Y. Arai, "Electronics and sensor study with the OKI SOI process," in *Proceedings of Topical Workshop on Electronics for Particle Physics*, 2007, pp. 57–63.

[71] ——, "Monolithic Pixel Detector with SOI Technology," 2011, presentation at AGH Krakow. [Online]. Available: http://rd.kek.jp/project/soi/

[72] K. Hara *et al.*, "Development of INTPIX and CNTPIX Silicon-On-Insulator Monolithic Pixel Devices," in *Proceedings of 19th International Workshop on Vertex Detectors 2010*, 2010. [Online]. Available: http://pos.sissa.it/archive/conferences/113/033/VERTEX\%202010_033.pdf

[73] F. Khalid, G. W. Deptuch *et al.*, "Monolithic Active Pixel Matrix with Binary Counters (mambo) ASIC," in *2010 IEEE Nuclear Science Symposium Conference Record (NSS/MIC)*, 2010, pp. 1544–1550.

[74] (2012) SOIPD Website. [Online]. Available: http://sirad.pd.infn.it/soipd/index.htm

[75] R. Ichimiya *et al.*, "Reduction techniques of the back gate effect in the SOI Pixel Detector," in *Proceedings of Topical Workshop on Electronics for Particle Physics 2009*, 2009, pp. 68–71.

[76] ORTEC, *DSPec50 and DSPec502*. [Online]. Available: http://www.ortec-online.com/Solutions/multichannel-analyzers.aspx

[77] F. Silveira, D. Flandre, and P. Jespers, "A gm/id Based Methodology for the Design of CMOS Analog Circuits and its Application to the Synthesis of a Silicon-on-Insulator Micropower OTA," *IEEE Journal of Solid State Circuits*, vol. 31, no. 9, pp. 1314–1319, 1996.

[78] S. Braibant *et al.*, "Investigation of design parameters for radiation hard silicon microstrip detectors," *Nucl. Instr. and Meth. in Phys. Research*, vol. A 485, pp. 343–361, 2002.

[79] E. Barberis *et al.*, "Capacitances in silicon microtrip detectors," *Nucl. Instr. and Meth. in Phys. Research*, vol. 342, pp. 90–95, 1994.

[80] A. Cerdeira and M. Estrada, "Analytical expressions for the calculation of pixel detector capacitances," *IEEE Trans. Nucl. Sci.*, vol. 44, no. 1, pp. 63–66, February 1997.

[81] Z. Y. Chang and W. M. C. Sansen, *Low-noise wide-band amplifiers in bipolar and CMOS technologies.* Norwell: Kluwer Academic Publishers, 1991.

[82] J. Oliver, D. Flandre, A. Kaiser, M. Valle, N. Barniol, O. Mocanu, and A. Uranga, *Low Power Techniques and Neural Applications.* Bellaterra, Spain: Centre de Visio per Computador Universitat Autonoma de Barcelona, 2002.

[83] J. C. Stanton, "A low power low noise amplifier for a 128 channel detector read-out chip," *IEEE Trans. Nucl. Sci.*, vol. 36, no. 1, pp. 522–527, 1989.

[84] Y. Hu, J. D. Berst, and M. Schaeffer, "A very low power consumption, low noise analog readout chip for capacitive detectors with a power supply of 3.3V," *Analog Integrated Circuits and Signal Processing*, vol. 17, pp. 249–260, 1998.

[85] M. A. Pavanello *et al.*, "Analog performance and application of graded-channel fully depleted SOI MOSFETs," *Solid-State Electronics*, vol. 44, no. 7, pp. 1219–1222, 2000.

[86] (2010) SOIPIX FY10-1 KEK/OKI SOI CMOS 0.20um MPW run (MX1413) website. [Online]. Available: http://rd.kek.jp/project/soi/cad10-1/

[87] Y. Arai, "Memo on IOBUF5M Library," 2010, layout library memo. [Online]. Available: http://rd.kek.jp/project/soi/cad10-1/sample/IOring_arai/IOBUF5Mreadme_v1.pdf

[88] ——, "IO Library for KEK Release Note (Ver.2)," 2009, IO library note. [Online]. Available: http://rd.kek.jp/project/soi/cad10-1/doc/08OEG31163_IOLib_KEK_ReleaseNote_v2.pdf

[89] Masao Okihara, "Report on SOI wafer PIN diodes / TEGs at test production," OKI Semiconductor Miyagi, Tech. Rep. 09HAC-1259, 2009. [Online]. Available: http://rd.kek.jp/project/soi/cad10-1/doc/09HAC-1259_FS2Y0-001JA_report_E.pdf

[90] OKI Semiconductor, "Development of 0.20um SOI Process for Pixel Sensor," 2010, presentation at SOIPIX Collaboration Meeting at Fermi National Laboratory.

[91] ——, "0.20um SOI CMOS LOGIC KEK PROCESS with 0.22um wiring drawing rule (rev. 14.0)," OKI Semiconductor Miyagi, Tech. Rep. QSD-11519, 2010. [Online]. Available: http://rd.kek.jp/project/soi/cad10-1/doc/KEK_3.3V022LDrawingRule_ver14_e.pdf

[92] ——, "0.2um SOI with 0.22um wiring process ï£¡for KEK circuit simulation parameter," OKI Semiconductor Miyagi, Tech. Rep. QSD-11523-0, 2010. [Online]. Available: http://rd.kek.jp/project/soi/cad10-1/spice/100723revise/QSD-11523-06_SPICE_param_e.pdf

[93] (2000) VLSI Projects by Jan David Schipper. [Online]. Available: http://www.nikhef.nl/~jds/

[94] C. Hu-Guo *et al.*, "A ten thousand frames per second readout MAPS for the EUDET beam telescope," in *Proceedings of the TWEPP 2009*, 2009, pp. 47–51. [Online]. Available: http://dx.doi.org/10.5170/CERN-2009-006.47

[95] ORTEC, "Introduction to amplifiers," Tech. Rep. [Online]. Available: www.ortec-online.com/download/Preamplifier-Introduction.pdf

[96] W. Kucewicz *et al.*, "Development of Monolithic Active Pixel Sensor in SOI Tehcnology fabricated on the wafer with thick device layer," in *2008 IEEE Nuclear Science Symposium Conference Record*, 2008, pp. 1123–1125.

[97] (2012) SOIPIX Collaboration. [Online]. Available: http://rd.kek.jp/project/soi/

[98] F. Khalid, "Monolithic Active pixel Matrix with Binary cOunters (MAMBO)," 2012, Presentation at PIXEL 2012.

[99] Y. Arai *et al.*, "Development of SOI pixel process technology," *Nucl. Instr. and Meth. in Phys. Research*, vol. 636, pp. S31–S36, 2012.

[100] Y. Arai, "Progress of SOI Pixel Process," 2012, Presentation at PIXEL 2012.

[101] ——, "Monolithic Pixel Detector with SOI technology," 2011, Presentation at CERN PH-ESE Electronics Seminar.

[102] M. Kochiyama *et al.*, "Radiation effects in silicon-on-insulator transistors with back-gate control method fabricated with OKI semiconductor 0.20mm FD-SOI technology," *Nucl. Instr. and Meth. in Phys. Research*, vol. 636, pp. S62–S67, 2011. [Online]. Available: http://dx.doi.org/10.1016/j.nima.2010.04.086

[103] P. Alvarez, L. S. Yee, and E. Cortina, "Irradiation Effects of a Monolithic Pixel sensor in FD-SOI Technology with 62 MeV-protons," in *Poster Presentation at IEEE Nuclear Science Symposium 2014*, 2014.

[104] Y. Ikegami *et al.*, "Evaluation of OKI SOI technology," *Nucl. Instr. and Meth. in Phys. Research*, vol. 579, no. 2, pp. 706–711, 2007. [Online]. Available: http://dx.doi.org/10.1016/j.nima.2007.05.272

[105] PV Education - Optical Properties of Silicon. [Online]. Available: http://pveducation.org/pvcdrom/materials/optical-properties-of-silicon

[106] LHC Outreach - Collisions. [Online]. Available: http://lhc-machine-outreach.web.cern.ch/lhc-machine-outreach/collisions.htm

[107] Y. Arai, "International review of the detector technology project. Part 1: SOI," 2013, http://rd.kek.jp/project/soi/publications.html.

[108] Y. Ono *et al.*, "Development of the Pixel OR SOI detector for high energy physics experiments," *Nucl. Instr. and Meth. in Phys. Research*, 2013. [Online]. Available: http://dx.doi.org/10.1016/j.nima.2013.06.044i

[109] M. Omodani *et al.*, "Development of Silicon-On-Insulator PHoton imaging array sensor (sophias) for X-ray Free-Electron Laser," 2012, Poster Presentation at the Pixel 2012.

[110] A. Ono *et al.*, "Design and evaluation of a soi pixel sensor for x-ray trigger driven readout," *IEEE Trans. Nucl. Sci.*, 2013. [Online]. Available: http://dx.doi.org/10.1109/TNS.2012.2225072

[111] Altera DE2 Development and Education Board. [Online]. Available: http://www.altera.co.uk/education/univ/materials/boards/de2/unv-de2-board.html

[112] N. Pacifico, I. D. Kittelmann, M. Fahrer, M. Moll, and O. Militaru, "Characterization of proton and neutron irradiated low resistivity p-on-n Magnetic Czochralski ministrip sensors and diodes," *Nucl. Instr. and Meth. in Phys. Research*, vol. A 658, pp. 55–60, 2011.

[113] L. S. Yee, A. Pin, O. Militaru *et al.*, "Test System for Charge Collection Efficiency Measurement SYCOC for Neutron Irradiated Silicon Sensors," in *Proceedings of 2nd International Conference on Advancements in Nuclear Instrumentation Measurement Methods and their Applications (ANIMMA)*, 2011, pp. 1–3.

[114] P. Alvarez, L. Soung Yee, E. Martin, E. Cortina, and C. Ferrer, "Characterization of SOI Monolithic Detector System," in *Proceedings of the PIXEL 2012*, 2012.